ANALOG CIRCUITS LABORATORY MANUAL

(R18A0483)

B.TECH
(II YEAR – II SEM)
(2020-21)

Prepared by:

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956

Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)

Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

ELECTRONICS & COMMUNICATION ENGINEERING

VISION

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

MISSION

To evolve into a center of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

QUALITY POLICY

- ❖ Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.
- ❖ Make the students experience the applications on quality equipment and tools.
- ❖ Provide systems, resources and training opportunities to achieve continuous improvement.
- ❖ Maintain global standards in education, training and services.

ROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1: PROFESSIONALISM & CITIZENSHIP

To create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with due consideration for ethical, ecological and economic issues.

PEO2: TECHNICAL ACCOMPLISHMENTS

To provide knowledge based services to satisfy the needs of society and the industry by providing hands on experience in various technologies in core field.

PEO3: INVENTION, INNOVATION AND CREATIVITY

To make the students to design, experiment, analyze, interpret in the core field with the help of other multi disciplinary concepts wherever applicable.

PEO4: PROFESSIONAL DEVELOPMENT

To educate the students to disseminate research findings with good soft skills and become a successful entrepreneur.

PEO5: HUMAN RESOURCE DEVELOPMENT

To graduate the students in building national capabilities in technology, education and research.

PROGRAMME SPECIFIC OBJECTIVES (PSOs)

PSO1

To develop a student community who acquire knowledge by ethical learning and fulfill the societal and industry needs in various technologies of core field.

PSO2

To nurture the students in designing, analyzing and interpreting required in research and development with exposure in multi disciplinary technologies in order to mould them as successful industry ready engineers/entrepreneurs

PSO3

To empower students with all round capabilities who will be useful in making nation strong in technology, education and research domains.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design / development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multi disciplinary environments.
12. **Life- long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Laboratory Rules

General Rules of Conduct in Laboratories:

1. You are expected to arrive on time and not depart before the end of a laboratory.

2. You must not enter a lab unless you have permission from a technician or lecturer.

3. You are expected to comply with instructions, written or oral, that the laboratory Instructor gives you during the laboratory session.

4. You should behave in an orderly fashion always in the lab.

5. You must not stand on the stools or benches in the laboratory.

6. Keep the workbench tidy and do not place coats and bags on the benches.

7. You must ensure that at the end of the laboratory session all equipment used is stored away where you found it.

8. You must put all rubbish such as paper outside in the corridor bins. Broken components should be returned to the lab technician for safe disposal.

9. You must not remove test equipment, test leads or power cables from any lab without permission.

10. Eating, smoking and drinking in the laboratories are forbidden.

11. The use of mobile phones during laboratory sessions is forbidden.

12. The use of email or messaging software for personal communications during laboratory sessions is forbidden.

13. Playing computer games in laboratories is forbidden.

Specific Safety Rules for Laboratories:

1. You must not damage or tamper with the equipment or leads.

2. You should inspect laboratory equipment for visible damage before using it. If there is a problem with a piece of equipment, report it to the technician or lecturer. DONOT return equipment to a storage area

3. You should not work on circuits where the supply voltage exceeds 40 volts without very specific approval from your lab supervisor. If you need to work on such circuits, you should contact your supervisor for approval and instruction on how to do this safely before commencing the work.

4. Always use an appropriate stand for holding your soldering iron.

5. Turn off your soldering iron if it is unlikely to be used for more than 10 minutes.

6. Never leave a hot soldering iron unattended.

7. Never touch a soldering iron element or bit unless the iron has been disconnected from the mains and has had adequate time to cool down.

8. Never strip insulation from a wire with your teeth or a knife, always use an appropriate wire stripping tool.

9. Shield wire with your hands when cutting it with a pliers to prevent bits of wire flying about the bench.

PART-I: ELECTRONIC CIRCUITS

CYCLE-I: SIMULATION USING MULTISIM

CYCLE-II: HARDWARE EXPERIMENTS

PART-II: PULSE CIRCUITS

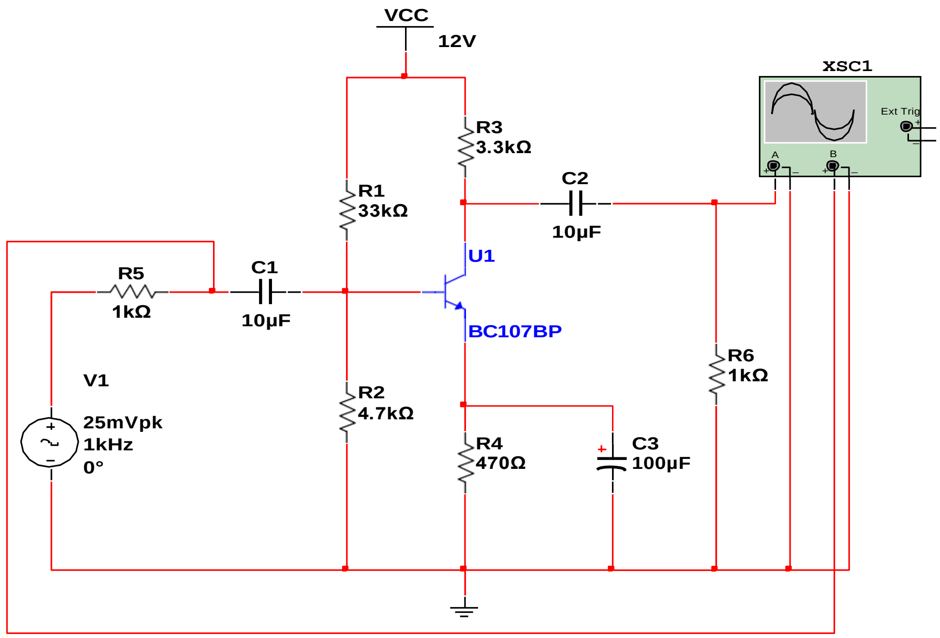
EXPERIMENT NO: 1
COMMON EMITTER AMPLIFIER

AIM:

To determine the gain and bandwidth of a CE Amplifier from its frequency response curve.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

The single stage common emitter amplifier circuit shown above uses what is commonly called "Voltage Divider Biasing" or "self biasing". This type of biasing arrangement uses two resistors as a potential divider network and is commonly used in the design of bipolar transistor amplifier circuits. This type of biasing arrangement greatly reduces the effects of varying Beta, (β) by holding the Base bias at a constant steady voltage. This type of biasing produces the greatest stability.

The Common Emitter Amplifier circuit has a resistor in its Collector circuit. The current flowing through this resistor produces the voltage output of the amplifier. The value of this resistor is chosen so that at the amplifiers quiescent operating point, Q-point this output voltage lies half way along the transistors load line. In Common Emitter Amplifier circuits, capacitors C1 and C2 are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not affected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component.

The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, CE is included in the Emitter leg circuit. This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only RL plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum.

Generally, the value of the bypass capacitor, CE is chosen to provide a reactance of at most, 1/10th the value of RE at the lowest operating signal frequency. A single stage Common Emitter Amplifier is also an "Inverting Amplifier" as an increase in Base voltage causes a decrease in V out and a decrease in Base voltage produces an increase in Vout. The output signal is 180° out of phase with the input signal.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the CE amplifier circuit i.e. Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.
5. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.
6. To observe the frequency response, go to simulate-----► analysis ►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.
7. A window opens showing the frequency response on the top and phase response at the bottom.
8. From the frequency response, calculate the bandwidth of the Amplifier.
9. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

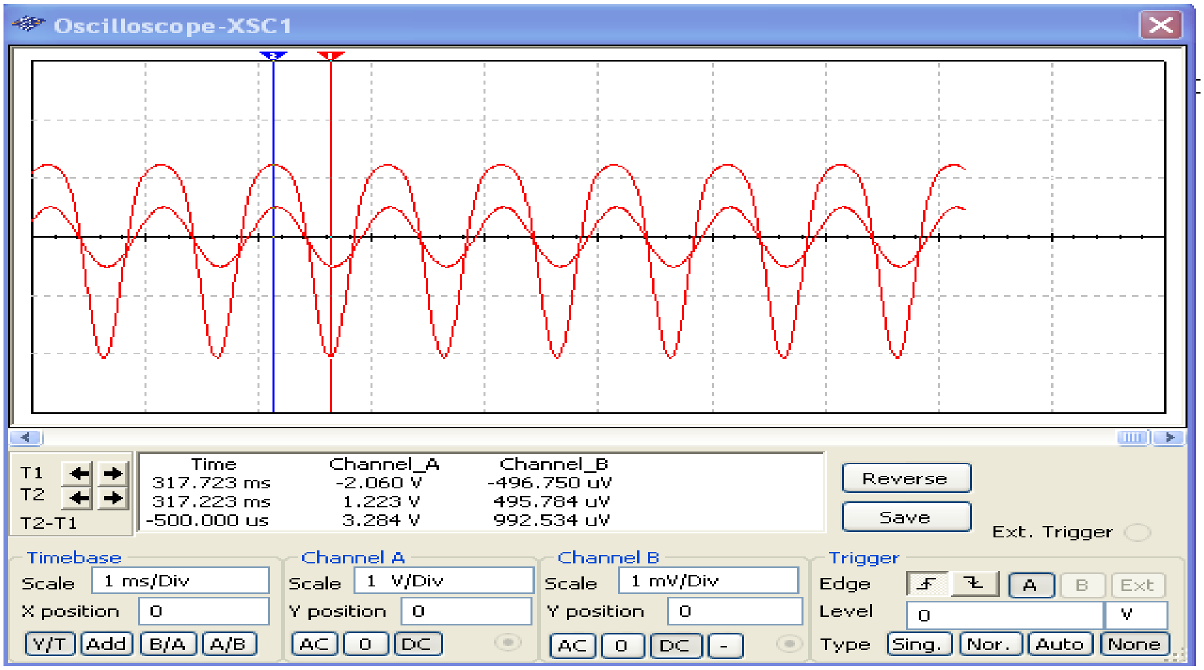
OBSERVATION TABLE:

S.No	Frequency(hz)	Output voltage(vo)	Voltage gain (vo/vi)	Gain (db) Avf=20 log (vo/vi).

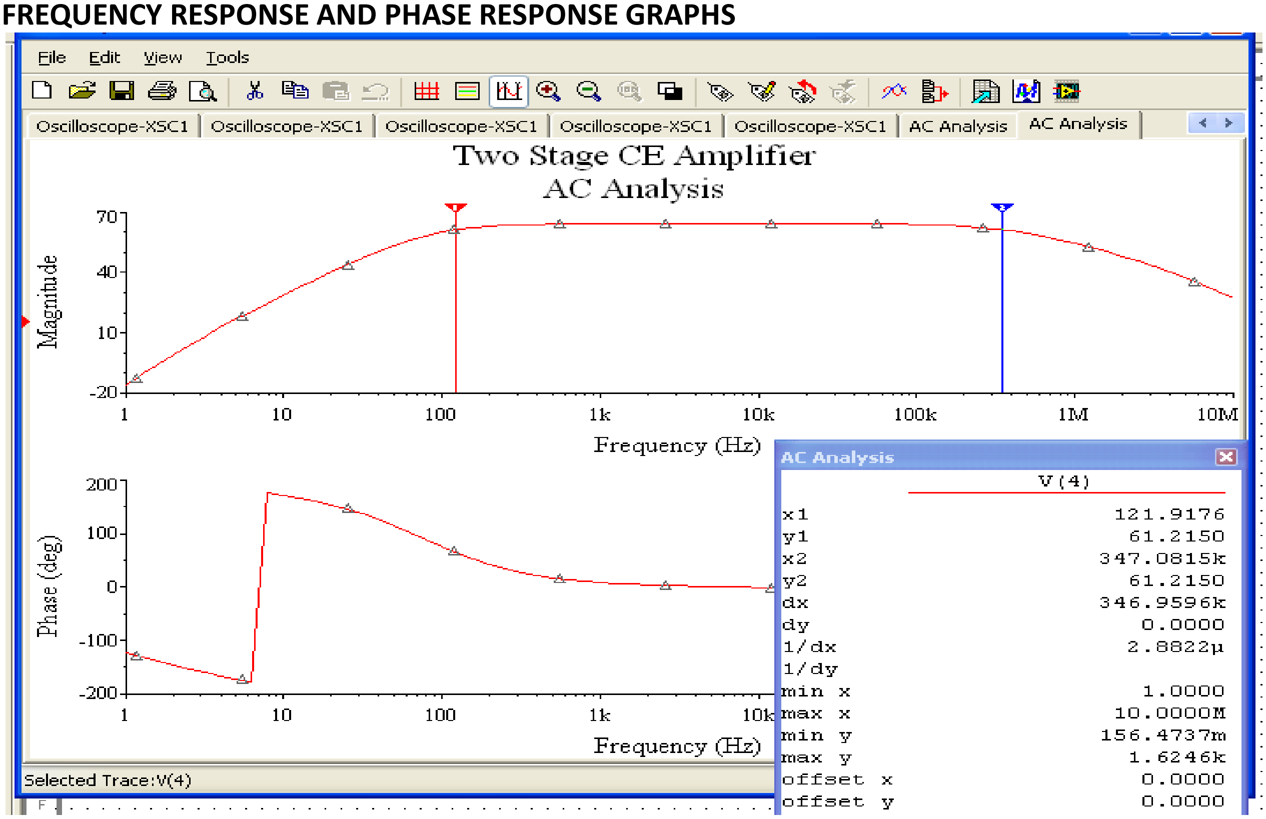
Bandwidth of the CE amplifier = f_h-f_l HZ

EXPECTED GRAPH:

INPUT Vs OUTPUT WAVEFORM



FREQUENCY RESPONSE AND PHASE RESPONSE GRAPHS



RESULT:

The maximum gain is_________dB and bandwidth is_________Hz of the CE Amplifier.

QUESTIONS:

1. What is the phase difference between input and output waveforms of CE amplifier?
2. What type of biasing is used in the given circuit?
3. If the given transistor is replaced by P-N-P, can we get the output or not?
4. What is the effect of emitter bypass capacitor on frequency response?
5. What is the effect of coupling capacitor?
6. What is the region of transistor so that it operates as an amplifier?
7. Draw the h-parameter model of CE amplifier.
8. How does transistor acts as an amplifier.
9. Mention the characteristics of CE amplifier.

Exercise Question:

1. Find the frequency response of CE Amplifier by changing the bypass capacitor value.
2. Find the frequency response of CE Amplifier by removing the bypass capacitor.

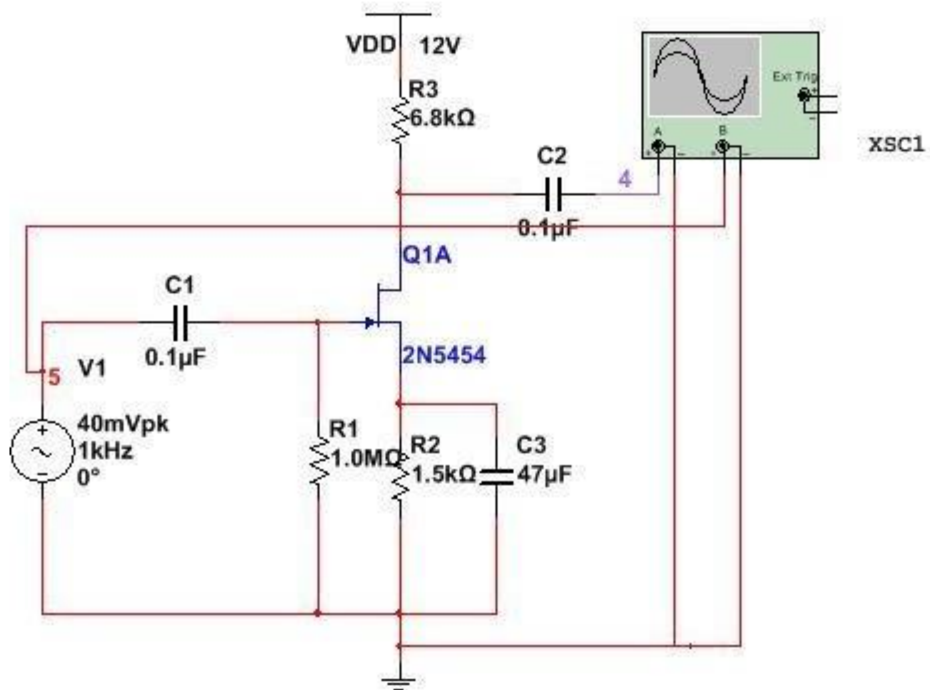
OBSERVATIONS:

EXPERIMENT NO: 2
COMMON SOURCE AMPLIFIER

AIM:
To determine the Band width from the frequency response of the common source FET Amplifier.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:
A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes.
In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P -N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate.

However, under some conditions there is a small current through the junction during part of the input signal cycle.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes. A common source amplifier FET amplifier has high input impedance and a moderate voltage gain. Also, the input and output voltages are 180 degrees out of Phase.

PROCEDURE:

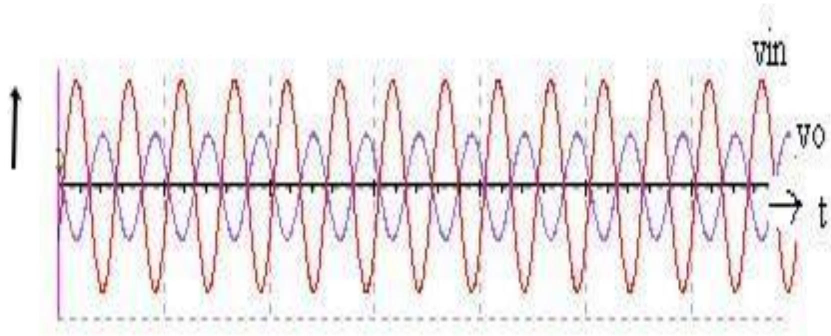
1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the CS FET amplifier circuit i.e. Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
3. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.
4. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.
5. To observe the frequency response, go to simulate-----► analysis ►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.
6. A window opens showing the frequency response on the top and phase response at the bottom.
7. From the frequency response, calculate the bandwidth of the Amplifier.
8. To obtain the netlist, go to transfer ---- ►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit containing the specifications of all the used components used in the design of the circuit.

OBSERVATION TABLE:

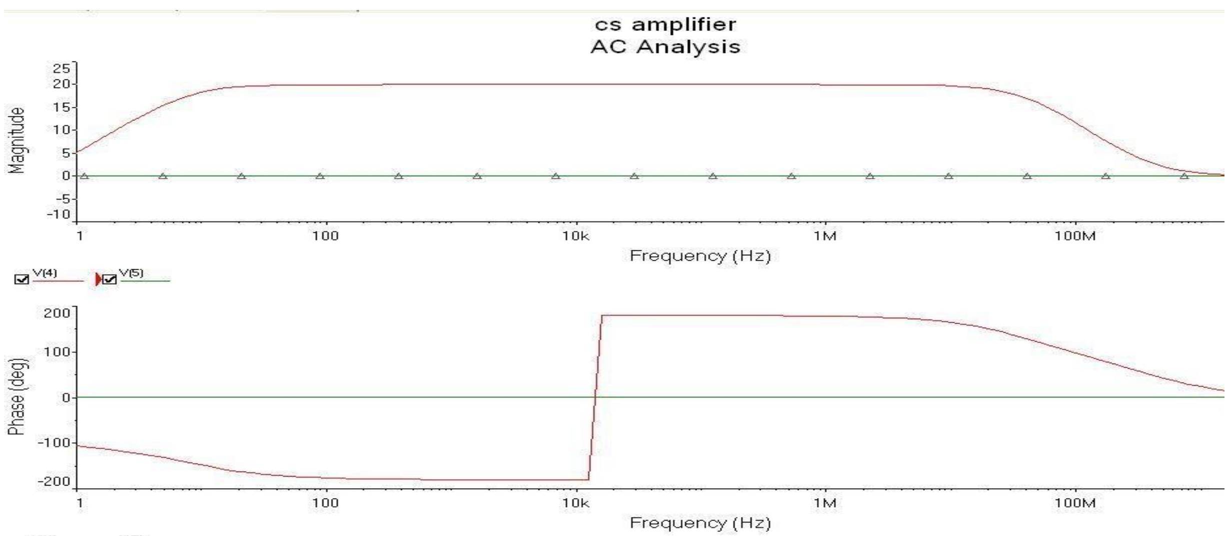
S.No	Frequency(hz)	Output voltage(vo)	Voltage gain (vo/vi)	Gain (db) Avf=20 log (vo/vi).

Bandwidth of the CE-CB Cascode amplifier=f_h___f_l Hz

MODEL GRAPH:
Input vs Output Waveforms



FREQUENCY RESPONSE:



RESULT: We have obtained the frequency response of the common Source FET Amplifier and also found its Bandwidth to be________Hz.

QUESTIONS:
1. How does FET acts as an amplifier?
2. What are the parameters of a FET?
3. What is an amplification factor?
4. Draw the h-parameter model of the FET.
5. What are the advantages of FET over BJT?
6. What is the region of FET so that it acts as an amplifier?
7. What are the differences between JFET and MOSFET?
8. What type of biasing is used in the given circuit?

Exercise Question:

1. Find the frequency response of CS Amplifier by changing the bypass capacitor value.
2. Find the frequency response of CS Amplifier by removing the bypass capacitor.

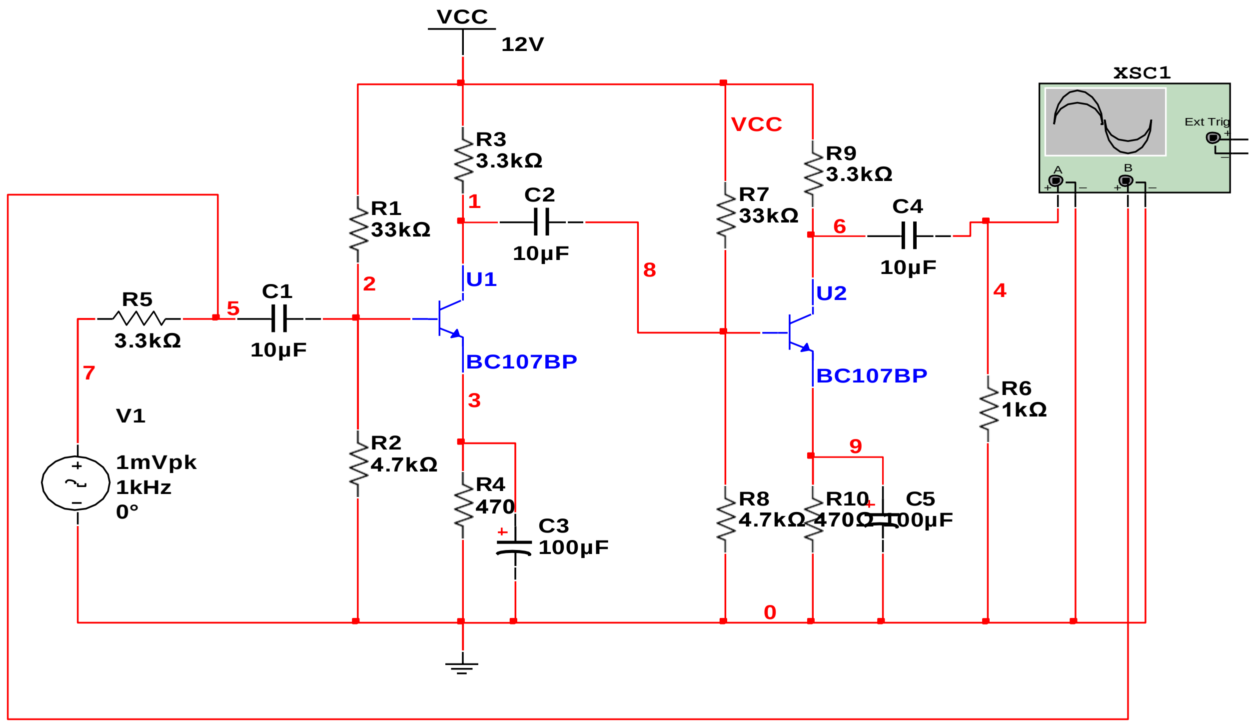
OBSERVATIONS:

EXPERIMENT NO: 3
TWO STAGE RC-COUPLED AMPLIFIER

AIM:
To study the response of a two stage RC-coupled amplifier and calculate gain and band width.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:
As the gain provided by a single stage amplifier is usually not sufficient to drive the load, so to achieve extra gain multi-stage amplifier are used. In multi-stage amplifiers output of one-stage is coupled to the input of the next stage. The coupling of one stage to another is done with the help of some coupling devices. If it is coupled by RC then the amplifier is called RC -coupled amplifier. Frequency response of an amplifier is defined as the variation of gain with respective frequency. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases. At low frequencies the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass through from one stage to the next stage.

APPLICATIONS:
1. Audio amplifiers
2. Radio Transmitters and Receivers.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the two stage RC Coupled amplifier circuit i.e. Resistors, Capacitors, Transistors.
3. Voltage sources, Power sources, Ground etc on the design window.
4. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
5. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.
6. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.
7. To observe the frequency response, go to simulate-----► analysis----- ►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.
8. A window opens showing the frequency response on the top and phase response at the bottom.
9. From the frequency response, calculate the bandwidth of the Amplifier.
10. To obtain the netlist, go to transfer ---- ►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

OBSERVATION TABLE:

S.No	Frequency(hz)	Output voltage(vo)	Voltage gain (vo/vi)	Gain (db) Avf=20 log (vo/vi).

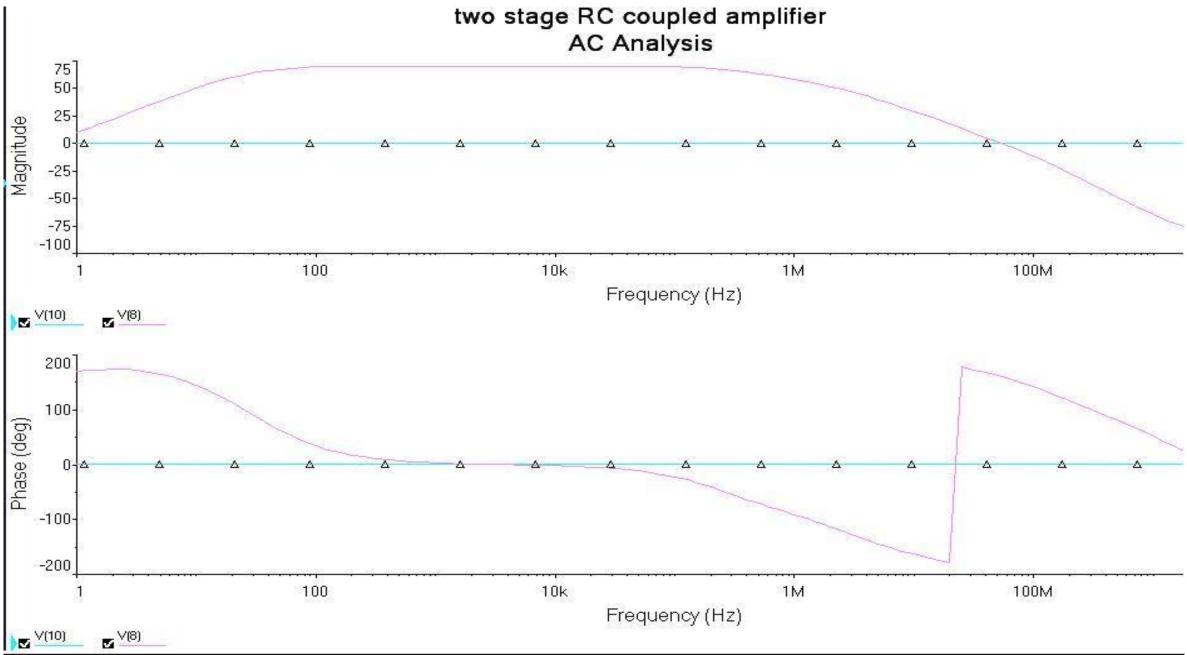
Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

CALCULATIONS:

1. Determine lower cut-off frequency and upper cut-off frequency from the graph.
2. Calculate Band width.

EXPECTED GRAPH:

Frequency Response:



RESULT:

The maximum gain is_________dB and bandwidth is_________Hz of the CE Amplifier**.**

QUESTIONS:

1. What are the advantages and disadvantages of multi-stage amplifiers?
2. Why gain falls at HF and LF?
3. Why the gain remains constant at MF?
4. Explain the function of emitter bypass capacitor, CE?
5. How the band width will be affected as more number of stages are cascaded?
6. Define frequency response?
7. Give the formula for effective lower cut-off frequency, when N-number of stages is cascaded.

Exercise Question:

Find the frequency response of 2 Stage CE Amplifier by changing the coupling capacitor to

i) Direct coupling
ii) Transformer coupling
iii)

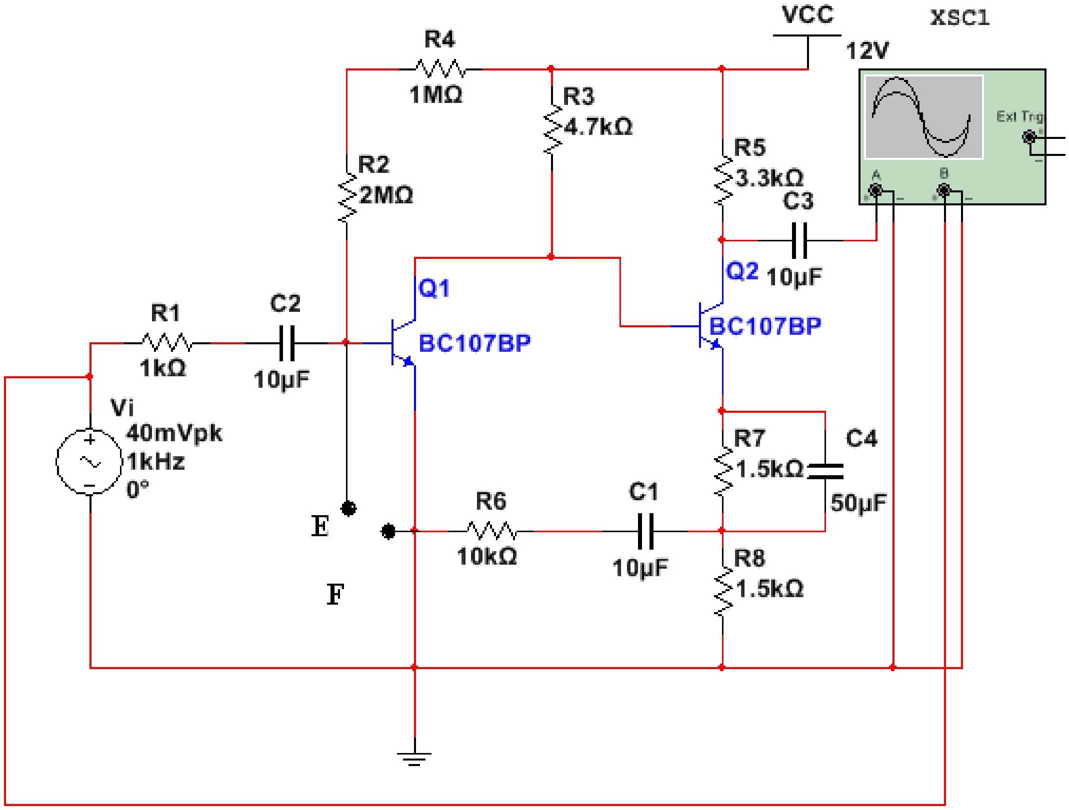
OBSERVATIONS:

EXPERIMENT NO: 4
CURRENT SHUNT FEEDBACK AMPLIFIER

AIM:
To determine the effect of feedback on the frequency response of a current shunt feedback amplifier.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



PROCEDURE:

TO DETERMINE THE FREQUENCY RESPONSE WITH FEEDBACK

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the current shunt feedback amplifier circuit i.e. Resistors, Capacitors, Diodes, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
3. Connect the channel of the Oscilloscope to the output of the circuit and by using the simulation switch and check output waveform.
4. To obtain the netlist, go to transfer ►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

5. Vary the input frequency from 10Hz to 1MHz with input voltage constant (40mvpp) and note down the output voltage.
6. Calculate the voltage gain in dB using the formula Av=20 log(Vo/Vi).

TO DETERMINE THE FREQUENCY RESPONSE WITH FEEDBACK

1. Now connect E-F terminals in the circuit.
2. Connect the output of the feedback amplifier to the other channel of the CRO.
3. Vary the input frequency from 10Hz to 1MHz with input voltage constant (40mvpp) and note down the output voltage.
4. Calculate the voltage gain in dB using the formula Av=20 log (Vo/Vi).

OBSERVATIONS TABLE

1. **WITHOUT FEEDBACK**

Vi= 40mvp-p at 1kHz

S.No	Frequency(hz)	Output voltage(vo)	Voltage gain (vo/vi)	Gain (db) Avf=20 log (vo/vi).

Bandwidth without feedback=------------

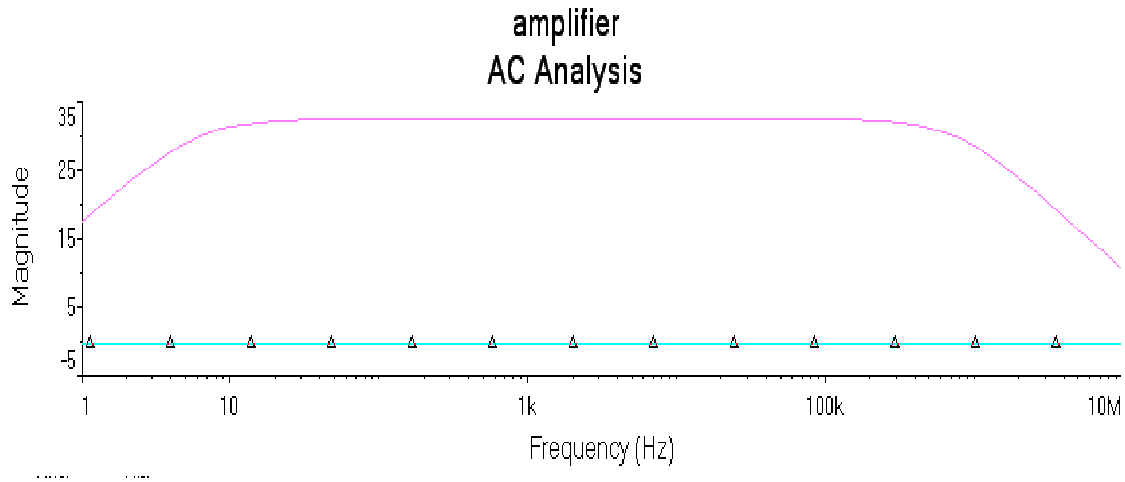
2. **WITH FEEDBACK**

Vi= 40mvp-p at 1kHz

S.NO	Frequency(hz)	Output voltage (vo)	Voltage gain (avf=vo/vi)	Gain (db) Avf=20 log (vo/vi).

Bandwidth with feedback = ------------

EXPECTED GRAPH:



RESULT:

The Av of the current shunt feedback amplifier is_____and the bandwidth is_________without feedback and The Av of the current shunt feedback amplifier is_____and the bandwidth is _______with feedback.

QUESTIONS:

1. What is feedback?
2. What are the characteristics of feedback?
3. What is meant by sampling and mixing?
4. What are the configurations of feedback amplifiers?
5. What is the effect of feedback on an amplifier?
6. What is the effect of feedback on input and output resistances?

Exercise Question:

1. Determine the input resistance ,Output resistance of Current Shut Feedback amplifier with and without feedback?

OBSERVATIONS:

EXPERIMENT NO: 5

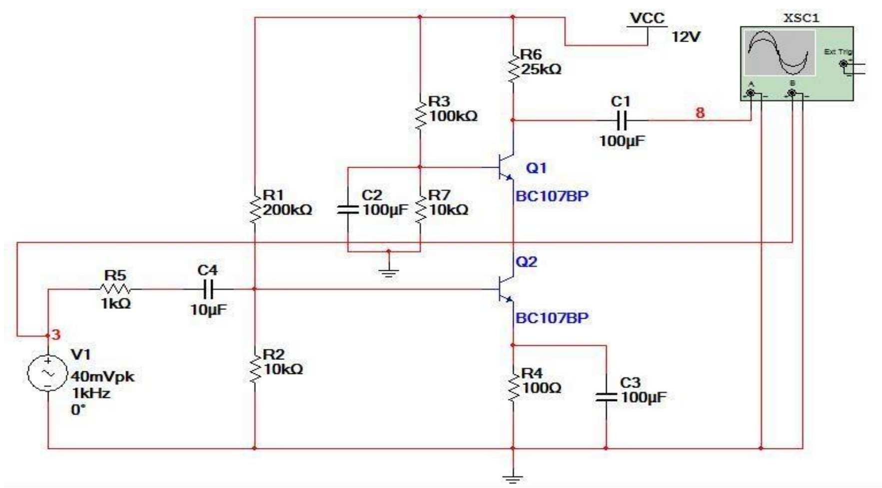
CE-CB CASCODE AMPLIFIER

AIM:

To determine the gain and bandwidth of a CE –CB Cascode Amplifier from its frequency response curve.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

A Cascode amplifier consists of a common-emitter stage loaded by the emitter of a common-base stage. While the C-B (common-base) amplifier is known for wider bandwidth than the C-E (common-emitter) configuration, the low input impedance (10s of Ω) of C-B is a limitation for many applications. The solution is to precede the C-B stage by a low gain C-E stage which has moderately high input impedance (kΩs). The stages are in a cascode configuration, stacked in series, as opposed to cascaded for a standard amplifier chain. The cascode amplifier configuration has both wide bandwidth and moderately high input impedance. Before the invention of the RF dual gate MOSFET, the BJT Cascode amplifier could have been found in UHF (ultra high frequency) TV tuners. A Cascode amplifier has a high gain, moderately high input impedance, high output impedance, and a high bandwidth.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the CE -CB cascode amplifier circuit i.e Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.
5. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.

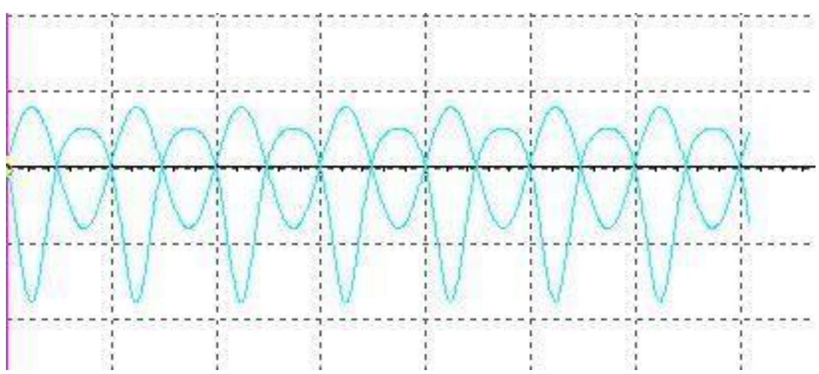
6. To observe the frequency response, go to simulate-----► analysis-----►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.
7. A window opens showing the frequency response on the top and phase response at the bottom.
8. From the frequency response, calculate the bandwidth of the Amplifier.
9. To obtain the net list, go to transfer ---- ►export netlist and save the net list in text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

OBSERVATION TABLE:

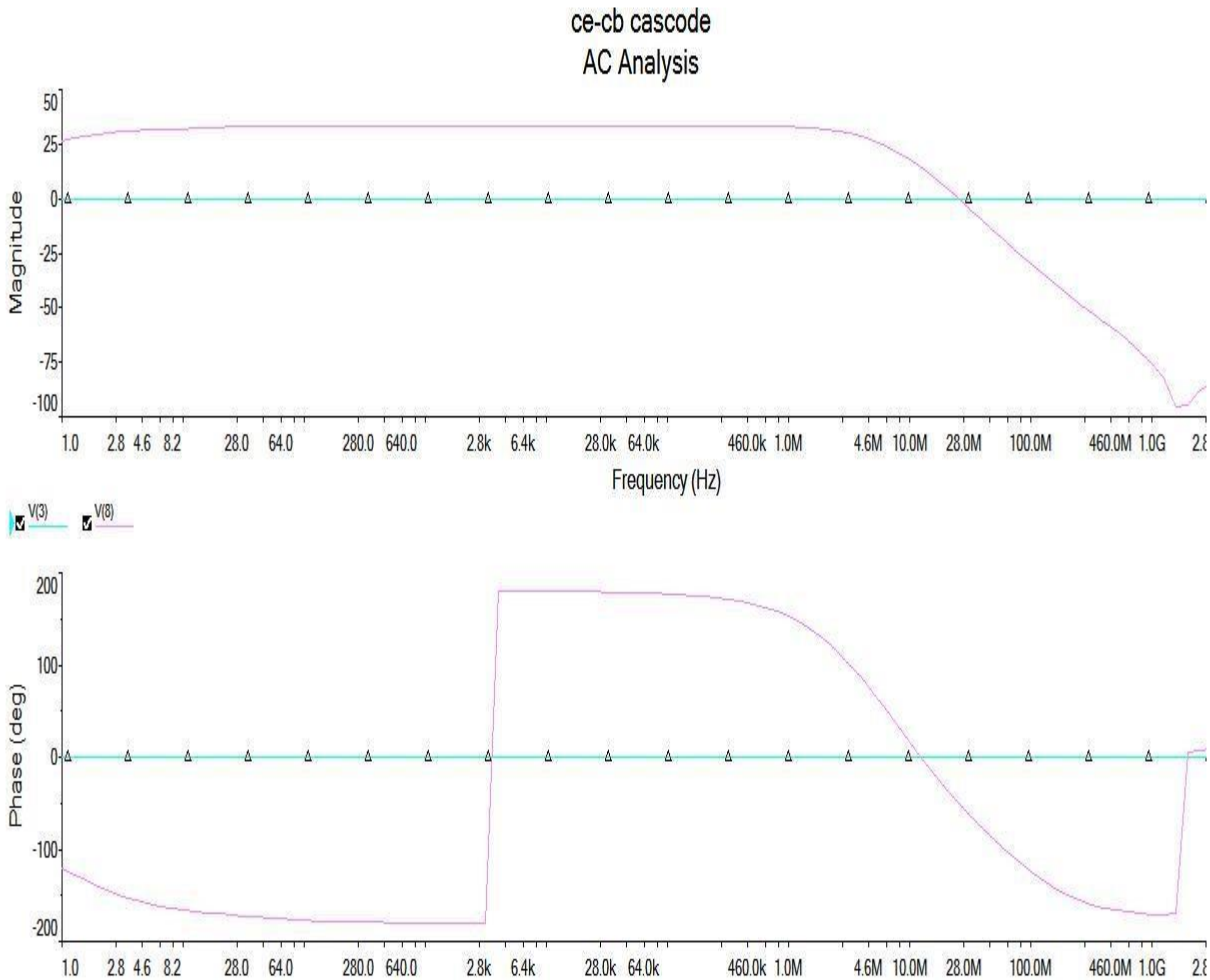
S.NO	FREQUENCY(Hz)	GAIN(dB)

Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

EXPECTED GRAPH:
Input Vs Output waveforms



REQUENCY RESPONSE AND PHASE RESPONSE GRAPHS



RESULT:

The maximum gain is_______dB and bandwidth is____________Hz of the CE - CB Cascode Amplifier.

QUESTIONS:

1. What is the difference between cascading and cascading?
2. What are the advantages of cascading?
3. What is the upper and lower cutoff frequencies of an n-stage cascaded amplifier?
4. What is the effective bandwidth of an n-stage Cascaded amplifier?
5. What is the preferred amplifier configuration for input stage in a cascade amplifier?

Exercise Question:

1. Observe the Frequency response and bandwidth of n Stage cascaded amplifier?

OBSERVATIONS:

EXPERIMENT NO: 6
RC PHASESHIFT OSCILLATOR

AIM:

To determine the frequency of oscillation of an RC Phase Shift Oscillator.

SOFTWARE REQUIRED: Multisim

DESIGN PROCEDURE:

a) Let R = 10K

$$fr = \frac{1}{2\pi Rc\sqrt{6+4K}} \quad whenK = \frac{Rc}{R}$$

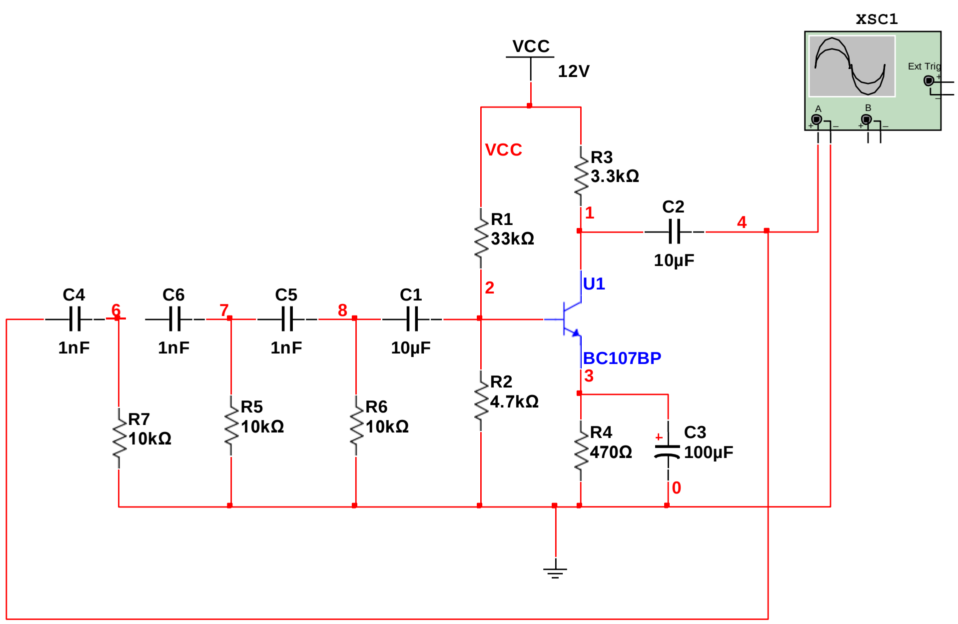
$$C = \frac{1}{2\pi \times 10K \times 6K\sqrt{6+4\times\frac{4K}{10K}}}$$

$$= 0.962nF \approx 1nF$$

$$\therefore R = 10K; C = 1nF$$

b) $hfe \geq 23 = \frac{29}{K} + 4K$

CIRCUIT DIAGRAM:

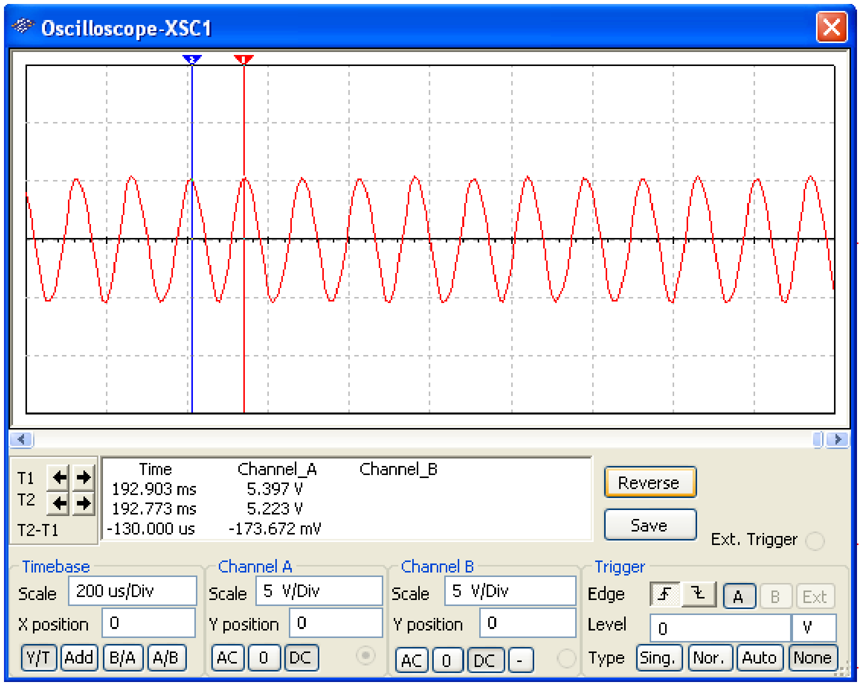


PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the RC Phase Shift Oscillator circuit i.e. Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect a frequency counter and click on the simulate button.
5. The frequency of oscillation will be displayed on the simulation window.

6. To obtain the netlist, go to transfer -----▶ export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

EXPECTED WAVEFORM:



RESULT: The frequency of oscillation of the RC Phase Shift Oscillator is______Hz.

QUESTIONS:

1. What is an Oscillator circuit?
2. What is the main difference between an amplifier and an oscillator?
3. State Barkhausen criterion for oscillation.
4. State the factors on which oscillators can be classified.
5. Give the expression for the frequency of oscillation and the minimum gain required for sustained oscillations of the RC phase shift oscillator.
6. Why three RC networks are needed for a phase shift oscillator? Can it be two or four?
7. What are the merits and demerits of phase shift oscillator?
8. At low frequency which oscillators are found to be more suitable?
9. What are the two important RC oscillators?

Exercise Question:

1. Find the frequency of oscillations by changing the feedback circuit component values shown below.

S.No	R(kΩ)	C(μF)	Theoretical frequency(KHz)	Practical frequency(KHz)
1	10	0.01		
2	10	0.022		
3	10	0.033		

OBSERVATIONS:

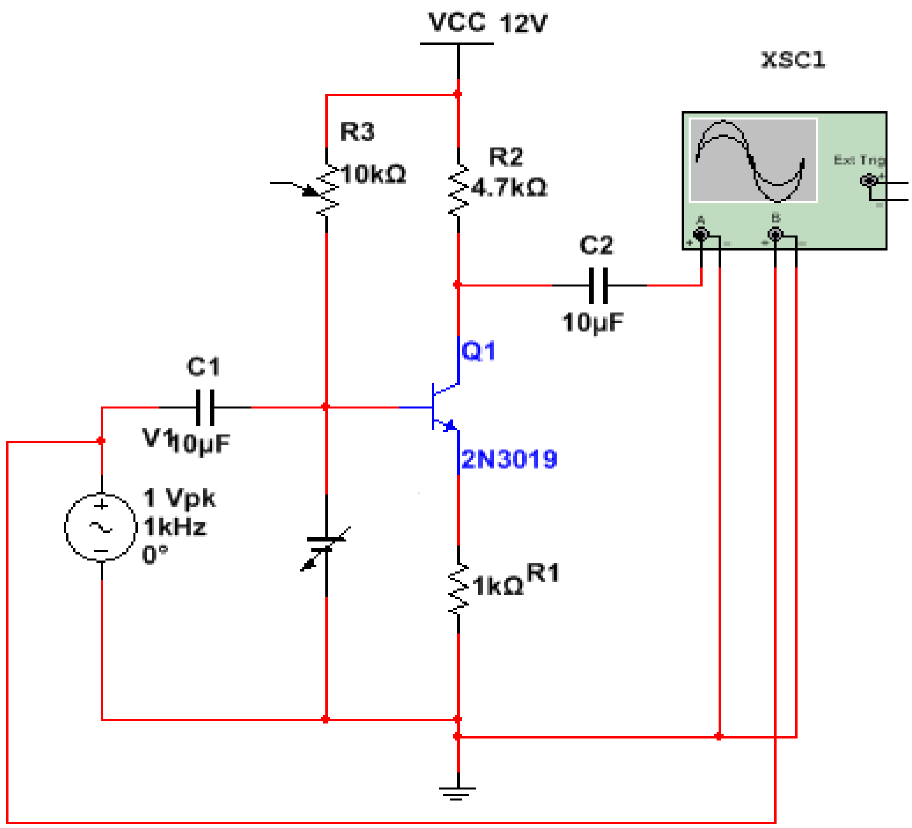
EXPERIMENT NO: 7
CLASS-A POWER AMPLIFIER

AIM:

To design a series fed class-A power amplifier in order to achieve max output ac power and efficiency.

EQUIPMENT REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

The above circuit is called as "series fed" because the load RL is connected in series with transistor output. It is also called as direct coupled amplifier.

ICQ = Zero signal collector current

VCEQ = Zero signal collector to emitter voltage

Power amplifiers are mainly used to deliver more power to the load. To deliver more power it requires large input signals, so generally power amplifiers are preceded by a series of voltage amplifiers. In class-A power amplifiers, Q-point is located in the middle of DC-load line. So output current flows for complete cycle of input signal. Under zero signal condition, maximum power dissipation occurs across the transistor. As the input signal amplitude increases power dissipation reduces The maximum theoretical efficiency is 25%.

APPLICATIONS:

This is used for low power linear applications in audio and wideband RF range, where high efficiency is not required.

EXTENSIONS:

In series fed class-A power amplifier we have calculated the efficiency i.e. how efficiently DC-power is converted into AC-power depending on the magnitude of input signal. Once we design a power amplifier for a particular efficiency, the circuit will not give that efficiency to all its input signals of different amplitudes. Hence, depending on the input signal we have to choose Vcc to obtain a particular efficiency. By employing Transformer coupling, efficiency can be improved to 50%.The experiment is conducted using low power transistors like BC107, SL100 only to get familiarity in biasing and measurement. Actual power amplifiers operate at 1 watt to 100 watts. This will call for operating transistors high current and small value resistors of greater than 1/4 to 1 watt which are used in the laboratory. Actual power amplifiers use heat sinks on the transistors.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the Complementary symmetry Class B Power amplifier circuit i.e. Resistors, Capacitors, Diodes, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect the channel of the Oscilloscope to the output of the circuit and by using the simulation switch and check output waveform.
5. To obtain the netlist, go to transfer ►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

OBSERVATIONS:

Efficiency is defined as the ratio of AC output power to DC input power

DC input power = $V_{cc} \times I_{CQ}$

AC output power = $V_{P-P}^2 / 8R_L$

CALCULATIONS:

Under zero signal condition:

$V_{cc} = I_B R_B + V_{BE}$

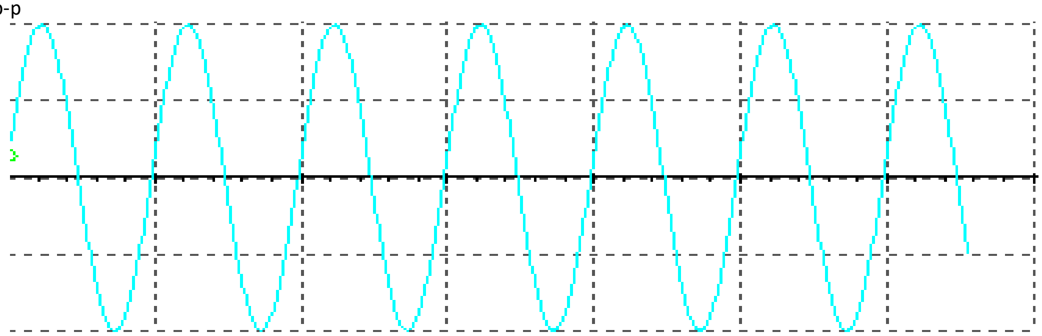
$I_{BQ} = (V_{cc} - V_{BE}) / R_B$

$I_{CQ} = \beta \times I_{BQ}$

$V_{CE} = V_{cc} - I_C R_C$

EXPECTED GRAPH:

Vin=$1V_{p-p}$



RESULT:

1. The maximum input signal amplitude which produces undistorted output signal is __________
2. The practical efficiency of the circuit is _________
3. The efficiency observed is _____________against theoretical maximum of 25%, Since ____________________

QUESTIONS:

1. Differentiate between voltage amplifier and power amplifier
2. Why power amplifiers are considered as large signal amplifier?
3. When does maximum power dissipation happen in this circuit?
4. What is the maximum theoretical efficiency?
5. Sketch wave form of output current with respective input signal.
6. What are the different types of class-A power amplifiers available?
7. What is the theoretical efficiency of the transformer coupled class-A power amplifier?
8. What is difference in AC, DC load line?
9. How do you locate the Q-point?
10. What are the applications of class-A power amplifier?

Exercise Question:

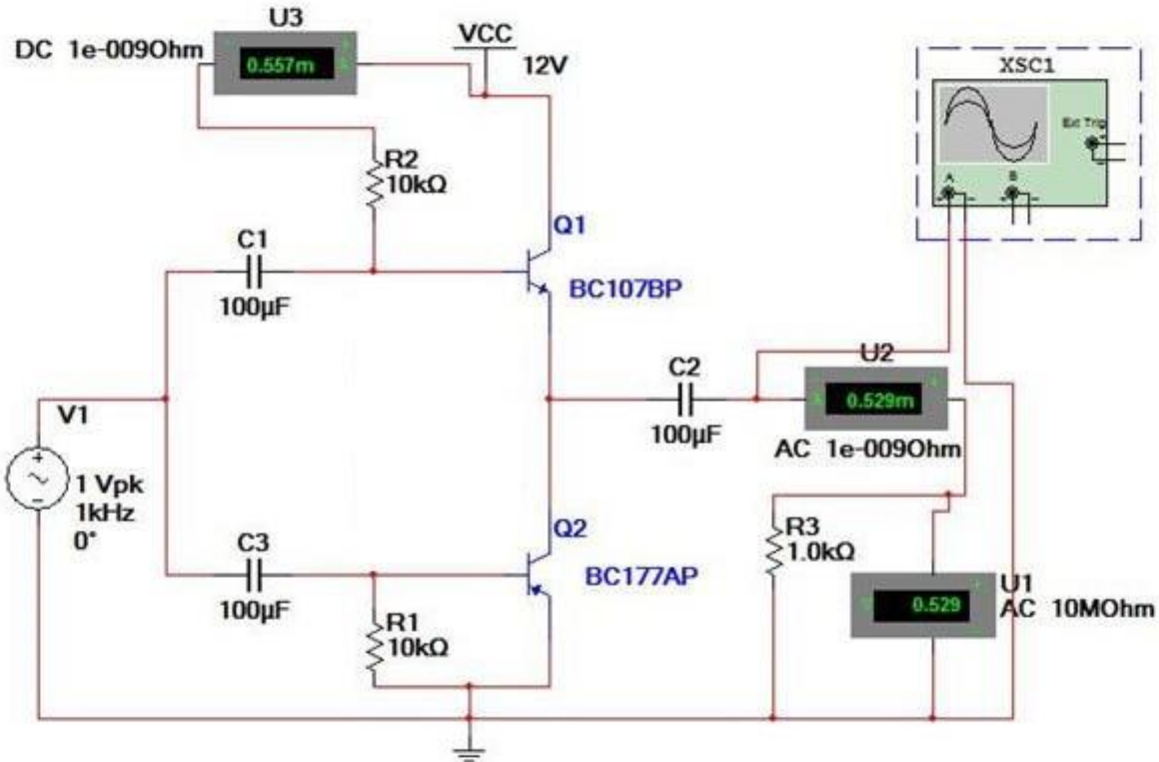
1. Try to increase the efficiency of Class A power amplifier using Transformer?

OBSERVATIONS:

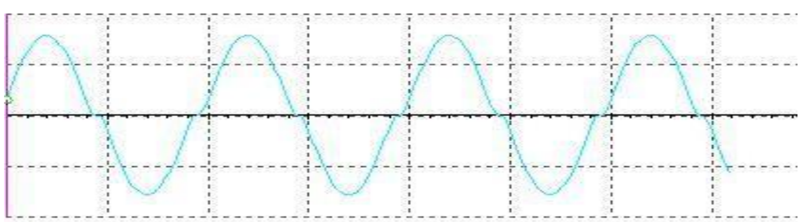
EXPERIMENT NO: 8
CLASS B COMPLEMENTARY SYMMETRY AMPLIFIER

AIM:
To find the efficiency of a Complementary symmetry Class B Power Amplifier.
SOFTWARE REQUIRED: Multisim
CIRCUIT DIAGRAM:

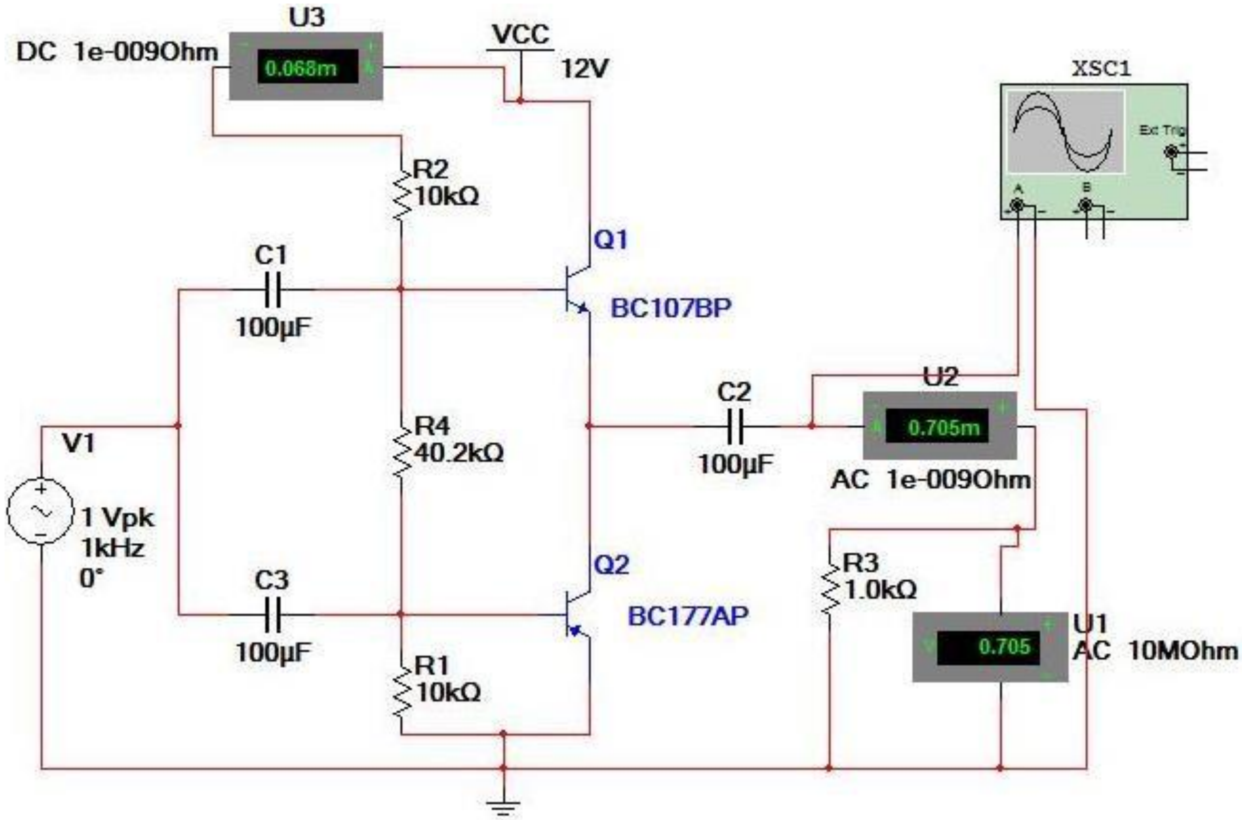
a) Complementary symmetry Class B Power Amplifier Circuit With crossover distortion



EXPECTED GRAPH:
Output waveform of Complementary symmetry Class B Power Amplifier Circuit with crossover distortion

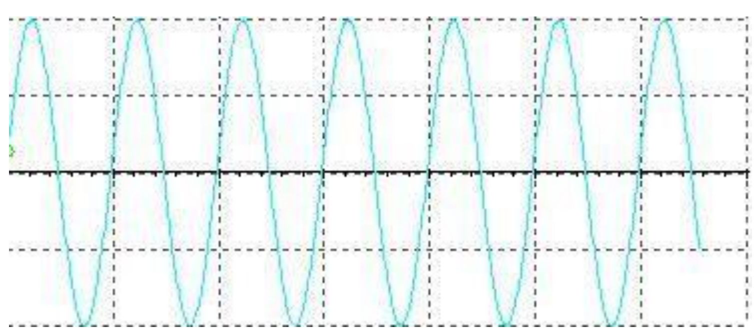


b) Class B Power Amplifier circuit Where crossover distortion is eliminated



EXPECTED GRAPH:

Output waveform of Complementary symmetry Class B Power Amplifier circuit where crossover distortion is eliminated



THEORY:

The Class B amplifier circuit above uses complimentary transistors for each half of the waveform and while Class B amplifiers have a much high efficiency than the Class A types, one of the main disadvantages of class B type push-pull amplifiers is that they suffer from an effect known commonly as Crossover Distortion.

It takes approximately 0.7 volts (measured from base to emitter) to get a bipolar transistor to start conducting. In a class B amplifier, the output transistors are not "pre -biased" to an "ON" state of operation. This means that the part of the output waveform which falls below this 0.7 volt window will not be reproduced accurately as the transition between the two transistors (when they are switching over from one to the other), the transistors do not stop or start conducting exactly at the zero crossover point even if they are specially matched pairs.

The output transistors for each half of the waveform (positive and negative) will each have a 0.7 volt area in which they will not be conducting resulting in both transistors being "OFF" at the same time.

A simple way to eliminate crossover distortion in a Class B amplifier is to add two small voltage sources to the circuit to bias both the transistors at a point slightly above their cut-off point.. However, it is impractical to add additional voltage sources to the amplifier circuit so pn-junctions are used to provide the additional bias in the form of silicon diodes.

We know that we need the base-emitter voltage to be greater than 0.7v for a silicon bipolar transistor to start conducting, so if we were to replace the two voltage divider biasing resistors connected to the base terminals of the transistors with two silicon Diodes, the biasing voltage applied to the transistors would now be equal to the forward voltage drop of the diode. These two diodes are generally called Biasing Diodes or Compensating Diodes and are chosen to match the characteristics of the matching transistors.

OBSERVATIONS:

THEORETICAL CALCULATIONS:

$$I_{CQ} = \frac{Vcc}{2\pi R_L}$$

$$P_{in}(D.C) = \frac{(Vcc)^2}{2\pi R_L}$$

$$P_{out}(A.C) = \frac{(V_{max} - V_{min}) \times (I_{max} - I_{min})}{8}$$

$$(I_{max} - I_{min}) = \frac{Vcc}{R_L}$$

$$(V_{max} - V_{min}) = V_{CC}$$

$$P_{out}(A.C) = \frac{V_{CC} \times V_{CC}}{8R_L} = \frac{V_{CC}^2}{8R_L}$$

$$\%efficiency = \frac{P_{out}(A.C)}{P_{in}(D.C)} \times 100 = \frac{\frac{V_{CC}^2}{8R_L}}{\frac{V_{CC}^2}{2\pi R_L}} \times 100 = \frac{\pi}{4} \times 100 = 78.5\%$$

PRACTICAL CALCULATIONS:

$$\%efficiency = \frac{P_{out}(A.C)}{P_{in}(D.C)} \times 100$$

$$= \frac{V_{ac} \times I_{ac}}{V_{CC} \times I_{DC}} \times 100$$

RESULT:

The efficiency of Complementary Symmetry Class B Power Amplifier is____%.

QUESTIONS:

1. Explain complementary and symmetry concept?
2. What is the conduction angle in class B operation?
3. What is the efficiency of class B power amplifier?
4. What is the formula for output power in class B power amplifier

Exercise Question:

1. Eliminate the crossover distortion in Class B Power amplifier using Diode?

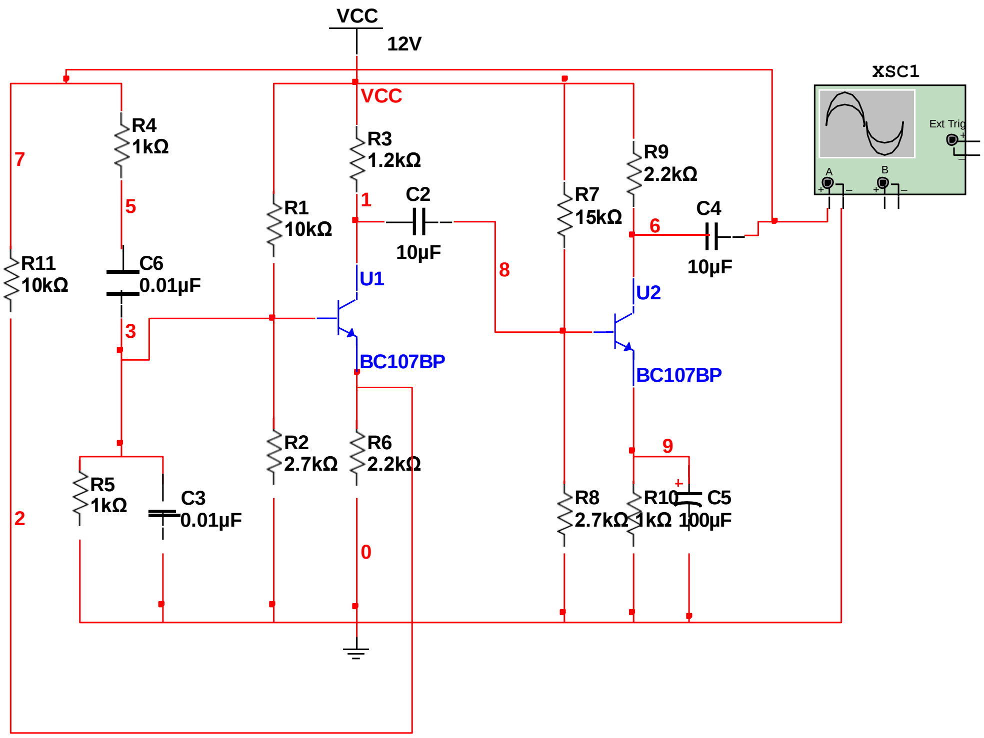
OBSERVATIONS:

EXPERIMENT NO: 9
WEIN BRIDGE OSCILLATOR

AIM:
To determine the frequency of oscillations of a Wien Bridge Oscillator using PSPICE or MULTISIM

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



EXPECTED GRAPH:

THEORY:

A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The oscillator is based on a bridge circuit originally developed by Max Wien in 1891 for the measurement of impedances. The bridge comprises four resistors and two capacitors. The oscillator can also be viewed as a positive gain amplifier combined with a band pass filter that provides positive feedback. Automatic gain control, intentional non-linearity and incidental non-linearity limit the output amplitude in various implementations of the oscillator.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the WEIN BRIDGE OSCILLATOR
3. Circuit i.e. Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.
4. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
5. Connect a frequency counter and click on the simulate button.
6. The frequency of oscillation will be displayed on the simulation window.
7. To obtain the netlist, go to transfer -----► export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

RESULT: The frequency of oscillation of the RC Phase Shift Oscillator is_______________Hz.

QUESTIONS:

1. Which components basically determine the frequency of oscillation in Wien Bridge Oscillator?
2. What is the expression for frequency of oscillation in Wien bridge oscillator?
3. What are the advantages of Wien bridge oscillator over turned L-C oscillators?
4. What are the typical applications of Wien bridge oscillator?

Exercise Question:

Find the frequency of oscillations by changing the bridge circuit component values shown below.

S.No	**R1 kΩ**	**R2 kΩ**	**C1(μF)**	**C2(μF)**	**Theoretical frequency(KHz)**	**Practical frequency(KHz)**
1	10	8.2	0.01	0.01		
2	10	8.2	0.022	0.022		
3	10	8.2	0.033	0.033		

OBSERVATIONS:

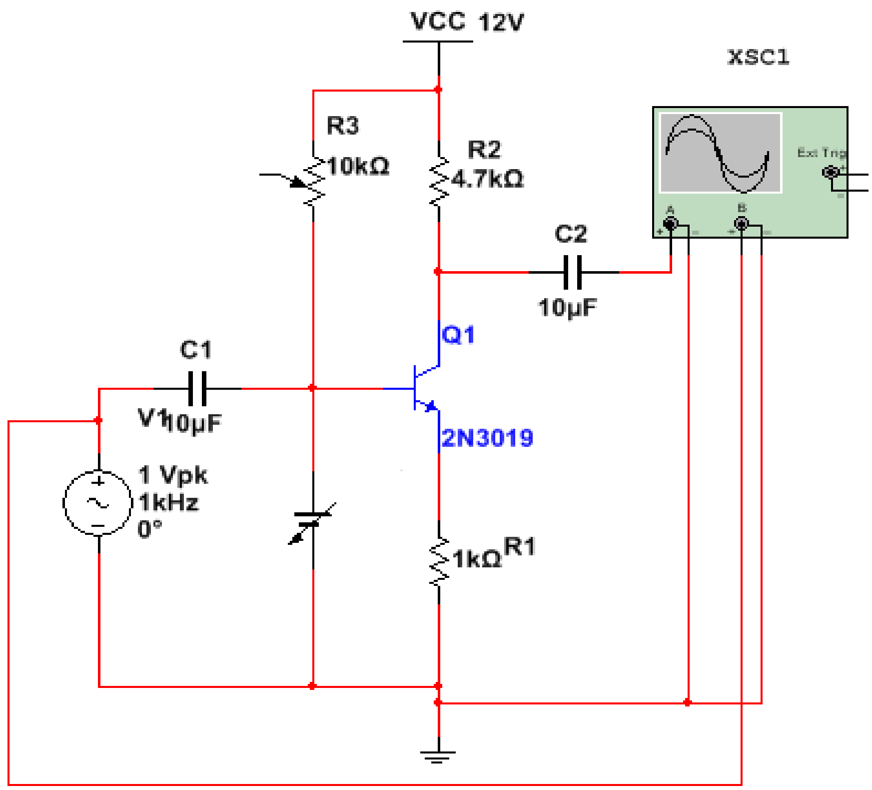
PART-II
HARDWARE EXPERIMENTS

EXPERIMENT NO: 1
CLASS-A POWER AMPLIFIER

AIM:
To design a series fed class-A power amplifier in order to achieve max output ac power and efficiency.

EQUIPMENT REQUIRED: Class-A power amplifier kit, C.R.O, Function Generator, Connecting probes.

CIRCUIT DIAGRAM:



THEORY:
The above circuit is called as "series fed" because the load R_L is connected in series with transistor output. It is also called as direct coupled amplifier.

I_{CQ} = Zero signal collector current

V_{CEQ} = Zero signal collector to emitter voltage

Power amplifiers are mainly used to deliver more power to the load. To deliver more power it requires large input signals, so generally power amplifiers are preceded by a series of voltage amplifiers. In class-A power amplifiers, Q-point is located in the middle of DC-load line. So output current flows for complete cycle of input signal. Under zero signal condition, maximum power dissipation occurs across the transistor. As the input signal amplitude increases power dissipation reduces The maximum theoretical efficiency is 25%.

APPLICATIONS:

This is used for low power linear applications in audio and wideband RF range, where high efficiency is not required.

EXTENSIONS:

In series fed class-A power amplifier we have calculated the efficiency i.e. how efficiently DC-power is converted into AC-power depending on the magnitude of input signal. Once we design a power amplifier for a particular efficiency, the circuit will not give that efficiency to all its input signals of different amplitudes. Hence, depending on the input signal we have to choose Vcc to obtain a particular efficiency. By employing Transformer coupling, efficiency can be improved to 50%.The experiment is conducted using low power transistors like BC107, SL100 only to get familiarity in biasing and measurement. Actual power amplifiers operate at 1 watt to 100 watts. This will call for operating transistors high current and small value resistors of greater than 1/4 to 1 watt which are used in the laboratory. Actual power amplifiers use heat sinks on the transistors.

PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Apply an input voltage of $1v_{p-p}$ at 1 KHz at input terminals of the circuit from the function generator.
3. Keep the input signal at constant frequency under mid frequency region and adjust the amplitude such that output voltage is undistorted and output current flows for 360^0
4. Calculate the power efficiency and compare it with theoretical efficiency.

OBSERVATIONS:

Efficiency is defined as the ratio of AC output power to DC input power

DC input power = $Vcc \times I_{CQ}$

AC output power = $V_{P-P}^2 / 8R_L$

CALCULATIONS:

Under zero signal condition:

$Vcc = I_B R_B + V_{BE}$

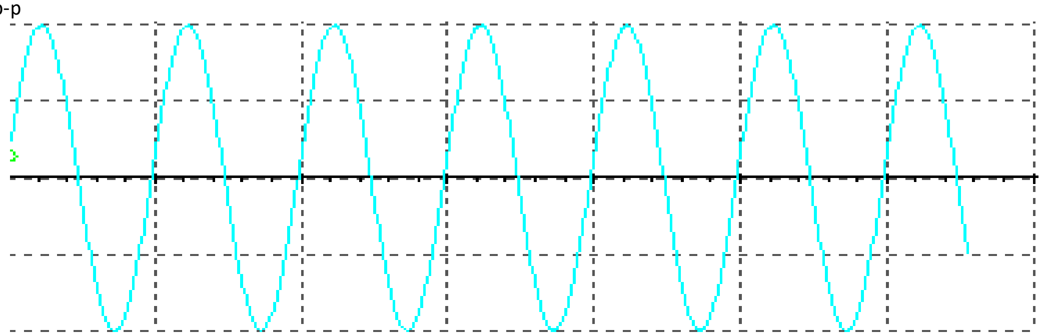
$I_{BQ} = (Vcc - V_{BE}) / R_B$

$I_{CQ} = \beta \times I_{BQ}$

$V_{CE} = Vcc - I_C R_C$

EXPECTED GRAPH:

Vin=$1V_{p-p}$



RESULT:

1. The maximum input signal amplitude which produces undistorted output signal is __________
2. The practical efficiency of the circuit is _________
3. The efficiency observed is_____________against theoretical maximum of 25%, since ____________________

QUESTIONS:

1. Differentiate between voltage amplifier and power amplifier
2. Why power amplifiers are considered as large signal amplifier?
3. When does maximum power dissipation happen in this circuit?
4. What is the maximum theoretical efficiency?
5. Sketch wave form of output current with respective input signal.
6. What are the different types of class-A power amplifiers available?
7. What is the theoretical efficiency of the transformer coupled class-A power amplifier?
8. What is difference in AC, DC load line?
9. How do you locate the Q-point?
10. What are the applications of class-A power amplifier?

Exercise Question:

1. Try to increase the efficiency of Class A power amplifier using Transformer?

OBSERVATIONS:

EXPERIMENT NO: 2
SINGLE TUNED VOLTAGE AMPLIFIER

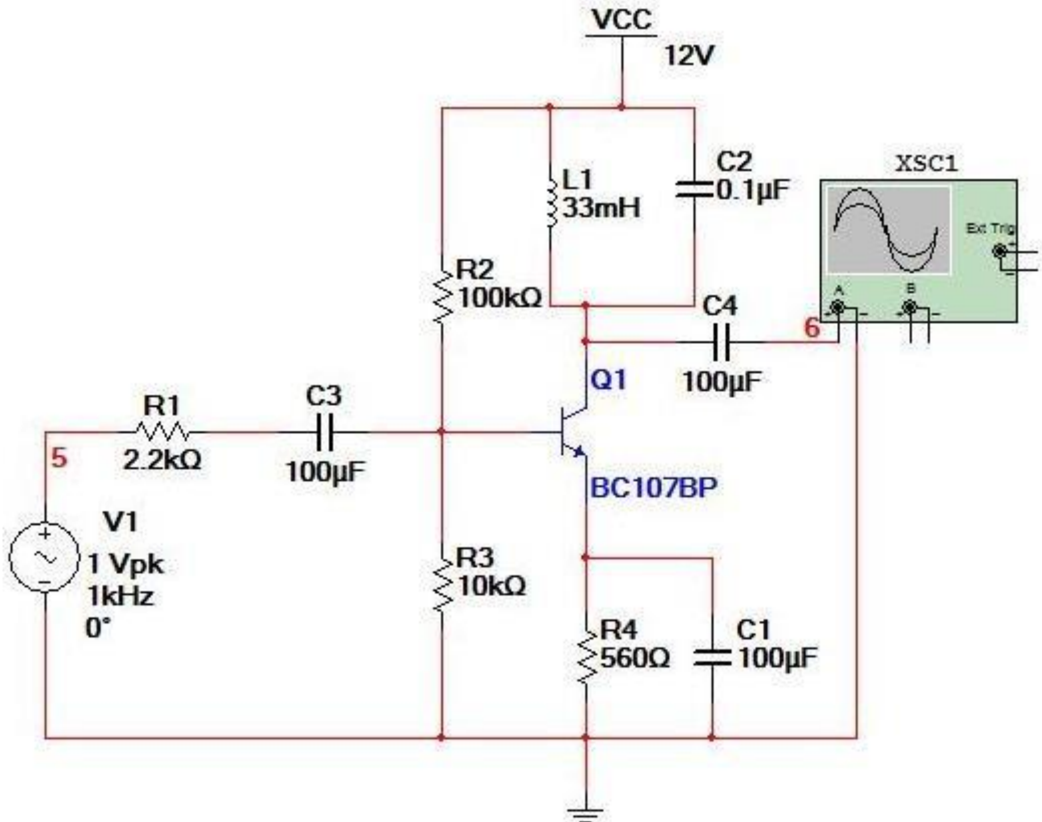
AIM:

To determine the resonant frequency and bandwidth of a tuned amplifier.

EQUIPMENT REQUIRED:

Tuned voltage amplifier kit, Function generator, CRO, connecting probes.

CIRCUIT DIAGRAM:



THEORY:

A tuned amplifier is one which uses one or more parallel tuned circuit as the load impedance. A tuned amplifier is capable of amplifying a signal over a narrow band of frequencies. The gain of a tuned amplifier is maximum at the resonant frequency and it falls sharply below and above the resonant frequency. At the resonant frequency, the inductive and capacitive reactances are equal.

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

PROCEDURE:

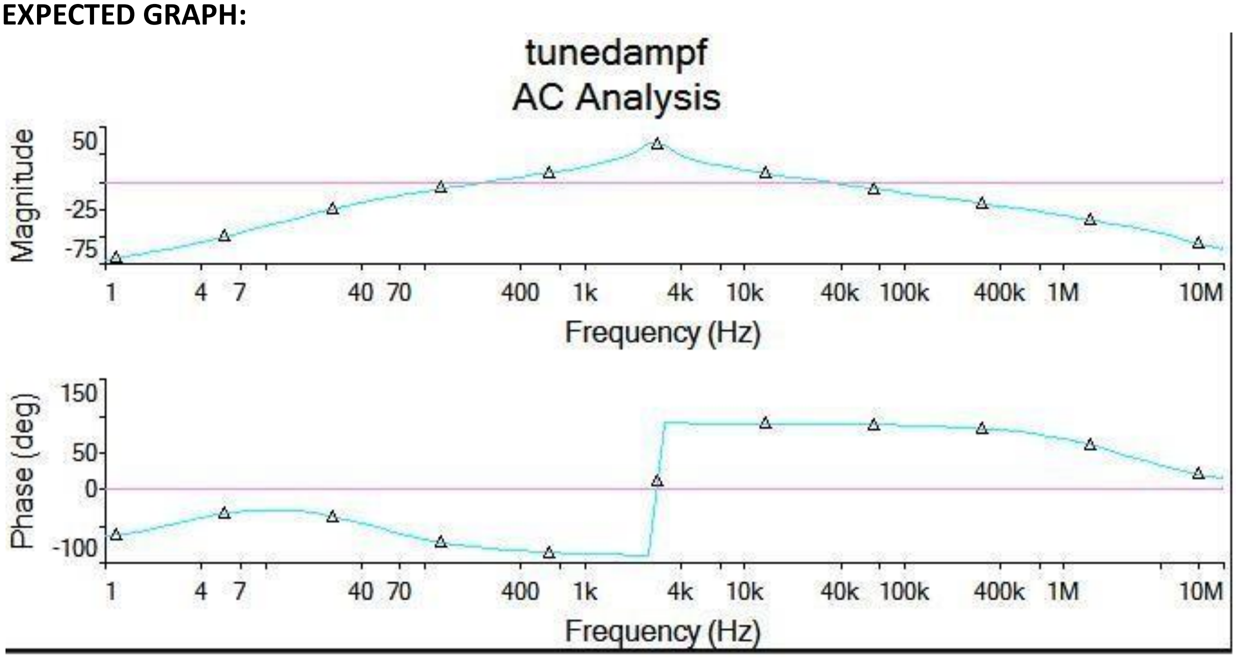
1. Apply an input voltage of 1vp -p at 1 kHz from the function generator at the input terminals of the Tuned voltage amplifier and observe the signal on the CRO.
2. Connect the output of the circuit to the channel of the CRO.
3. Note down the output voltage.
4. Calculate the voltage gain in dB using the formula Av=20 log (Vo/Vi).

OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (Vo)	VOLTAGE GAIN (Avf=Vo/Vi)	GAIN (dB) Avf=20 log (Vo/Vi).

Bandwidth of the CE amplifier = f_h-f_l HZ

EXPECTED GRAPH:



RESULT:

The maximum gain is________dB, the resonant frequency is________Hz and bandwidth is ________________Hz of the Tuned Amplifier.

QUESTIONS:

1. What is a tuned amplifier?
2. What is the formula for resonant frequency of a tuned amplifier?
3. What is the difference between single, double and stagger tuned amplifiers?

Exercise Question:

1. By changing the tuned circuit components set the center frequency to 10 Khz

OBSERVATIONS:

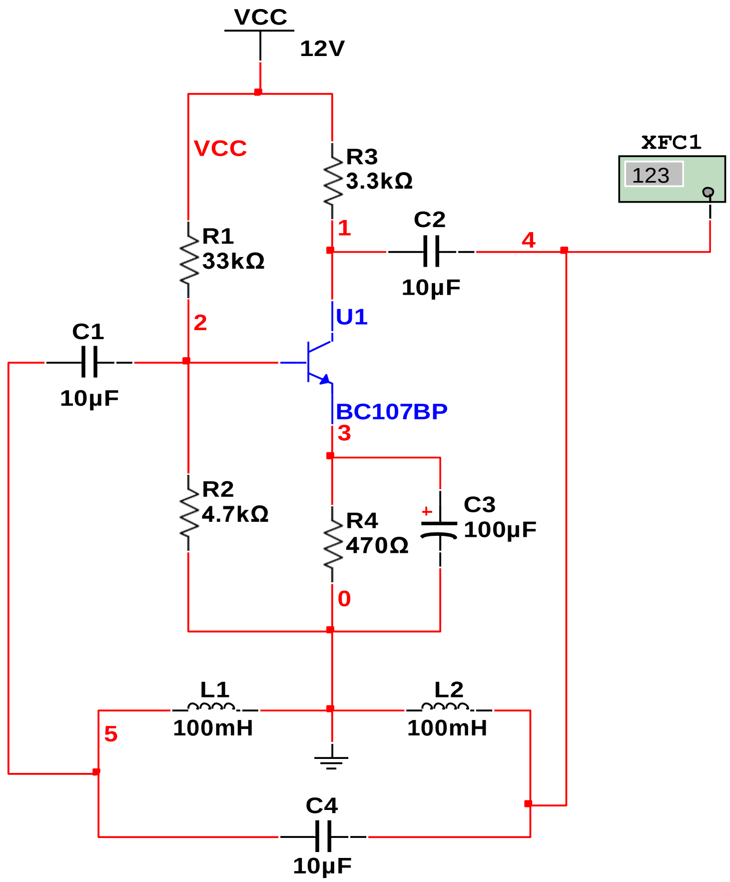
EXPERIMENT NO: 3 (A)
HARTLEY OSCILLATOR

AIM:

To determine the frequency of oscillations of the Hartley oscillator

EQUIPMENT REQUIRED: Hartley Oscillator kit, CRO, Connecting probes.

CIRCUIT DIAGRAM:



THEORY:

The Hartley oscillator is distinguished by a tank circuit consisting of two series-connected coils in parallel with a capacitor, with the feedback signal needed for oscillation taken from the center connection between the coils; the coils act as a voltage divider. The Hartley oscillator is the dual of the Colpitts oscillator which uses a voltage divider made of two capacitors rather than two inductors. Although there is no requirement for there to be mutual coupling between the two coil segments, the circuit is usually implemented using a tapped coil, with the feedback taken from the tap, as shown here. The optimal tapping point (or ratio of coil inductances) depends on the amplifying device used, which may be a bipolar junction transistor, FET, triode, or amplifier of almost any type (non-inverting in this case, although variations of the circuit with an earthed centre-point and feedback from an inverting amplifier or the collector/drain of a transistor are also common), but a Junction FET (shown) or triode is often employed as a good degree of amplitude stability (and thus distortion reduction) can be achieved with a simple grid leak resistor-capacitor combination in series with the gate or grid (see the Scott circuit below) thanks to diode conduction on signal peaks building up enough negative bias to limit amplification. The frequency of oscillation is approximately the resonant frequency of the tank circuit. If the capacitance of the tank capacitor is C and the total inductance of the tapped coil is L then

$$f = \frac{1}{2\pi\sqrt{LC}}$$

If two *uncoupled* coils of inductance L_1 and L_2 are used then

$$L = L_1 + L_2$$

However if the two coils are magnetically coupled the total inductance will be greater because of mutual inductance

$$L = L_1 + L_2 + k\sqrt{L_1 L_2}$$

The actual oscillation frequency will be slightly lower than given above, because of parasitic capacitance in the coil and loading by the transistor.

Advantages of the Hartley oscillator include:

1. The frequency may be adjusted using a single variable capacitor, one side of which can be earthed
2. The output amplitude remains constant over the frequency range
3. Either a tapped coil or two fixed inductors are needed, and very few other components
4. Easy to create an accurate fixed-frequency Crystal oscillator variation by replacing the capacitor with a (parallel-resonant) quartz crystal or replacing the top half of the tank circuit with a crystal and grid-leak resistor (as in the Tri-set oscillator).

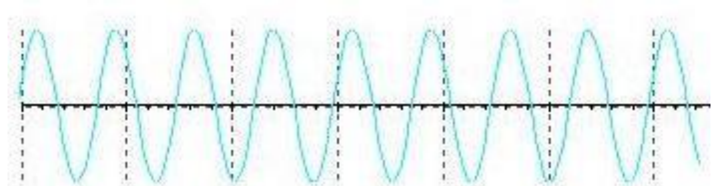
Disadvantages include:

Harmonic-rich output if taken from the amplifier and not directly from the LC circuit (unless amplitude -stabilization circuitry is employed).

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Connect the output of the Hartley Oscillator kit to the CRO.
3. Observe the sinusoidal signal as an output and note down the time period of the oscillation.
4. Compare the practical frequency with the theoretical frequency.

EXPECTED GRAPH:



OBSERVATIONS:

i. Theoretical frequency of oscillation:

L1=L2=C=

$$L = L_1 + L_2$$
$$f = \frac{1}{2\pi\sqrt{LC}}$$

ii. Practical frequency of oscillation:

T=_____

fo=1/ T= ___________Hz

RESULT:

The theoretical and practical frequency of oscillation of the Hartley Oscillator is calculated as _________and___________.

Exercise Question:

Find the frequency of oscillations by changing the feedback circuit component values shown below.

S.No	**L1 mH**	**L2 mH**	**C1(µF)**	**Theoretical frequency(KHz)**	**Practical frequency(KHz)**
1	5	5	0.01		
2	5	5	0.022		
3	5	5	0.033		

OBSERVATIONS:

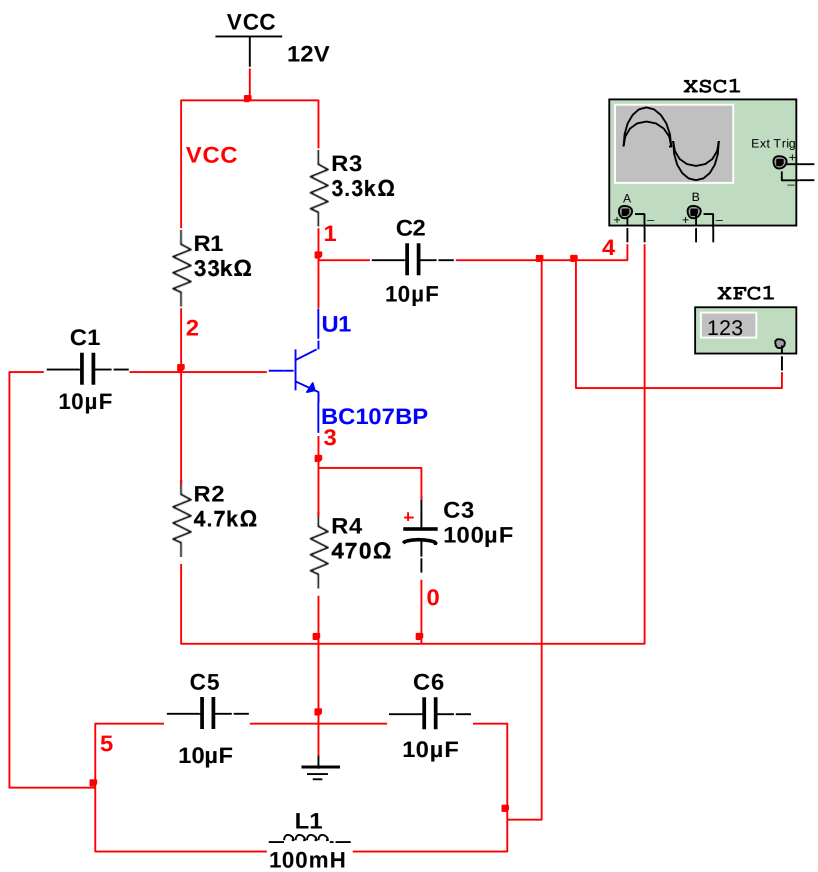
EXPERIMENT NO: 3 (B)
COLPITTS OSCILLATOR

AIM:

To determine the frequency of oscillation of a Colpitts Oscillator

EQUIPMENT REQUIRED: Colpitts Oscillator kit, CRO, Connecting probes

CIRCUIT DIAGRAM:



THEORY:

The Colpitts circuit, like other LC oscillators, consists of a gain device (such as a bipolar junction transistor, field effect transistor, operational amplifier, or vacuum tube) with its output connected to its input in a feedback loop containing a parallel LC circuit (tuned circuit) which functions as a bandpass filter to set the frequency of oscillation. Colpitts oscillator is the electrical dual of a Hartley oscillator, where the feedback signal is taken from an "inductive" voltage divider consisting of two coils in series (or a tapped coil). Fig. 1 shows the common-base Colpitts circuit. L and the series combination of C1 and C2 form the parallel resonant tank circuit which determines the frequency of the oscillator. The voltage across C2 is applied to the base-emitter junction of the transistor, as feedback to create oscillations. Here the voltage across C1 provides feedback. The frequency of oscillation is approximately the resonant frequency of the LC circuit, which is the series combination of the two capacitors in parallel with the inductor.

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1+C_2}\right)}}$$

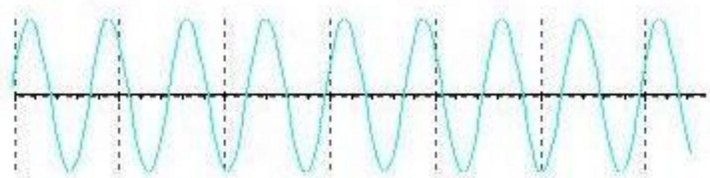
The actual frequency of oscillation will be slightly lower due to junction capacitances and resistive loading of the transistor.

As with any oscillator, the amplification of the active component should be marginally larger than the attenuation of the capacitive voltage divider, to obtain stable operation. Thus, a Colpitts oscillator used as a variable frequency oscillator (VFO) performs best when a variable inductance is used for tuning, as opposed to tuning one of the two capacitors. If tuning by variable capacitor is needed, it should be done via a third capacitor connected in parallel to the inductor (or in series as in the Clapp oscillator).

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Connect the output of the Colpitts Oscillator kit to the CRO.
3. Observe the sinusoidal signal as an output and note down the time period of the oscillation.
4. Compare the practical frequency with the theoretical frequency.

EXPECTED GRAPH:



OBSERVATIONS:

I. THEORETICAL FREQUENCY OF OSCILLATION:

C1=C2=L=

II. PRACTICAL FREQUENCY OF OSCILLATION:

T= ______

f_o =1/ T=____________Hz

RESULT:

The theoretical and practical frequency of oscillation of the Colpitts Oscillator is calculated as __________and____________.

QUESTIONS:

1. What is an Oscillator?
2. What is the main difference between an amplifier and an oscillator?
3. State Barkhausen criterion for oscillation.
4. State the factors on which oscillators can be classified.
5. What are the factors which contribute to change in frequency in oscillators?

Exercise Question:

Find the frequency of oscillations by changing the feedback circuit component values shown below.

S.No	L (mH)	C1(μF)	C2(μF)	Theoretical frequency(KHz)	Practical frequency(KHz)
1	5	0.01	0.01		
2	5	0.01	0.022		
3	5	0.01	0.033		

OBSERVATIONS:

EXPERIMENT NO: 4
COMMON SOURCE AMPLIFIER

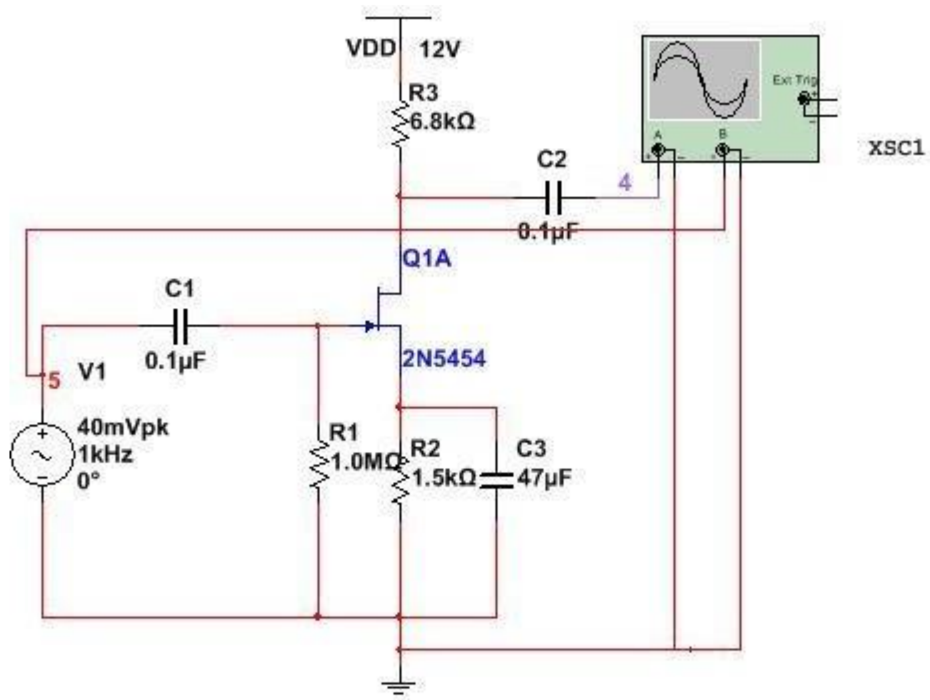
AIM:

To determine the Band width from the frequency response of the common source FET Amplifier.

SOFTWARE REQUIRED:

Common source hardware kit, function generator, CRO, Connecting probes

CIRCUIT DIAGRAM:



THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes.

In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P -N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.
Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes. A common source amplifier FET amplifier has high input impedance and a moderate voltage gain. Also, the input and output voltages are 180 degrees out of Phase.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the CS FET amplifier circuit i.e. Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.

3Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.

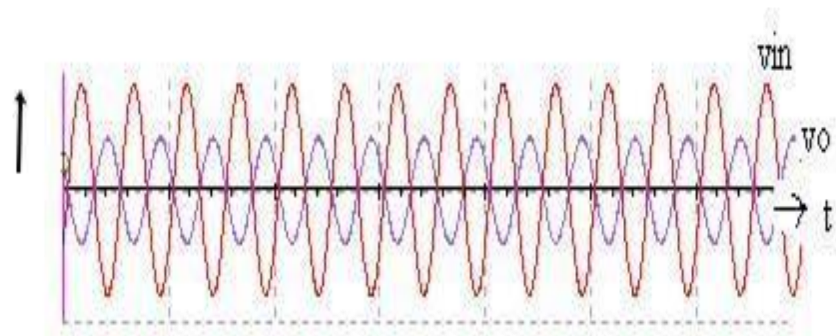
4. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.
5. To observe the frequency response, go to simulate-----► analysis ►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.
6. A window opens showing the frequency response on the top and phase response at the bottom.
7. From the frequency response, calculate the bandwidth of the Amplifier.
8. To obtain the netlist, go to transfer ---- ►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit containing the specifications of all the used components used in the design of the circuit.

OBSERVATION TABLE:

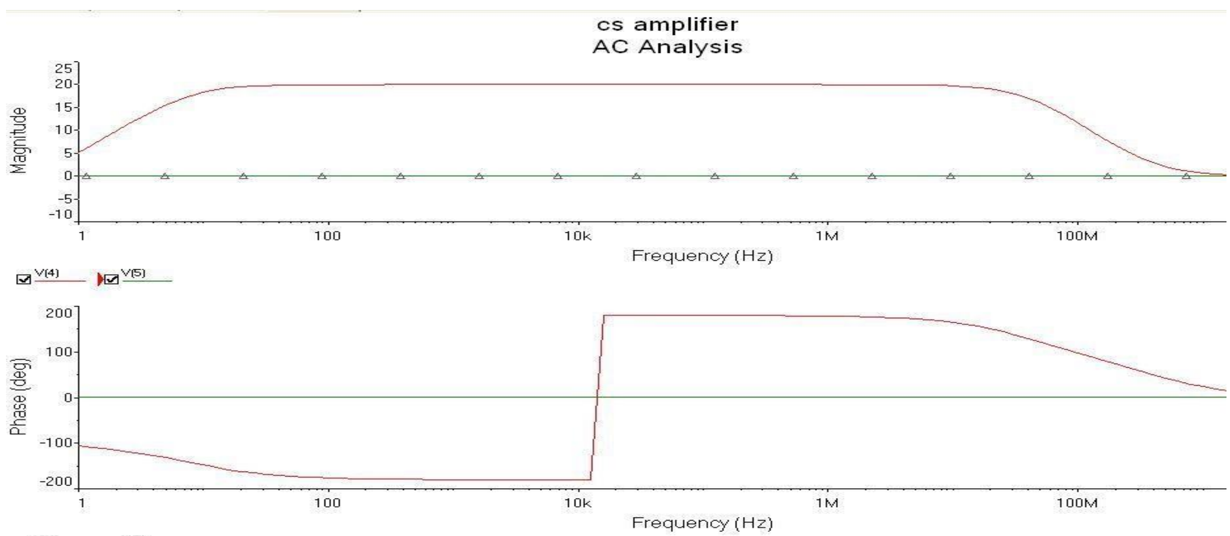
S.No	Frequency(hz)	Output voltage(vo)	Voltage gain (vo/vi)	Gain (db) Avf=20 log (vo/vi).

Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

MODEL GRAPH:
Input vs Output Waveforms



FREQUENCY RESPONSE:



RESULT: We have obtained the frequency response of the common Source FET Amplifier and also found its Bandwidth to be________Hz.

QUESTIONS:

1. How does FET acts as an amplifier?
2. What are the parameters of a FET?
3. What is an amplification factor?
4. Draw the h-parameter model of the FET.
5. What are the advantages of FET over BJT?
6. What is the region of FET so that it acts as an amplifier?
7. What are the differences between JFET and MOSFET?
8. What type of biasing is used in the given circuit?

Exercise Question:

1. Find the frequency response of CS Amplifier by changing the bypass capacitor value.
2. Find the frequency response of CS Amplifier by removing the bypass capacitor.

OBSERVATIONS:

EXPERIMENT NO-1
LINEAR WAVE SHAPING

AIM:

i) To observe the response of the designed low pass RC circuit for the given square waveform for T<<RC, T=RC and T>>RC.

ii) To observe the response of the designed high pass RC circuit for the given square waveform For T<<RC, T=RC and T>>RC.

APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	1KΩ,10 KΩ,100 KΩ	1
2	Capacitors	0.01µF	1
3	CRO	20MHz	1
4	Function generator	1MHz	1
5	Connecting Wires		As Required

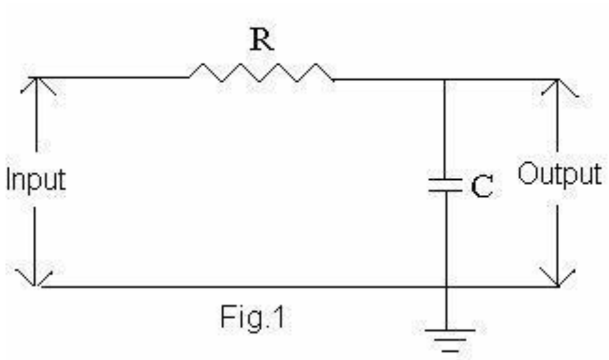
THEORY:

The process whereby the form of a non sinusoidal signal is altered by transmission through a linear network is called "linear wave shaping". An ideal low pass circuit is one that allows all the input frequencies below a frequency called cutoff frequency f_c and attenuates all those above this frequency. For practical low pass circuit (Fig.1) cutoff is set to occur at a frequency where the gain of the circuit falls by 3 dB from its maximum at very high frequencies the capacitive reactance is very small, so the output is almost equal to the input and hence the gain is equal to 1. Since circuit attenuates low frequency signals and allows high frequency signals with little or no attenuation, it is called a high pass circuit.

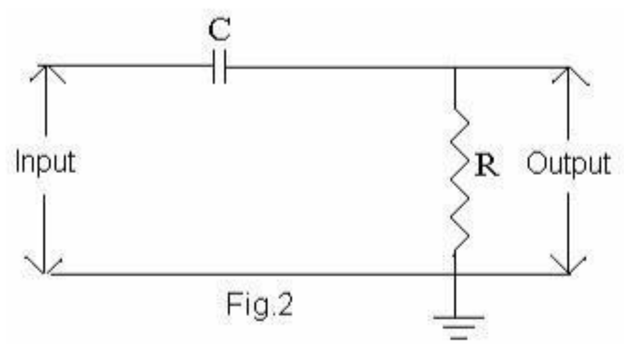
In high pass RC circuit, if the time constant is very small in comparison with the time required for the input signal to make an appreciable change, the circuit is called a "**Differentiator**". Under these circumstances the voltage drop across R will be very small in comparison with the drop across C. Hence we may consider that the total input Vi appears across C. So that the current is determined entirely by the capacitor. In low pass circuit, if the time constant is very large in comparison with the time required for the input signal to make an appreciable change, the circuit is called an "integrator". Under these circumstances the voltage drop across C will be very small in comparison to the drop across R and almost the total input Vi appears across R.

CIRCUIT DIAGRAM:

LOW PASS RC CIRCUIT:



HIGH PASS RC CIRCUIT:



PROCEDURE:

1. Connect the circuit as shown in figure (fig.1.1 and fig 1.2).
2. Apply the Square wave input to this circuit (Vi = 2 VP-P, f = 1KHz)
3. Observe the output waveform for (a) RC = T, (b) RC<<T, (c) RC>>T
4. Verify the values with theoretical calculations

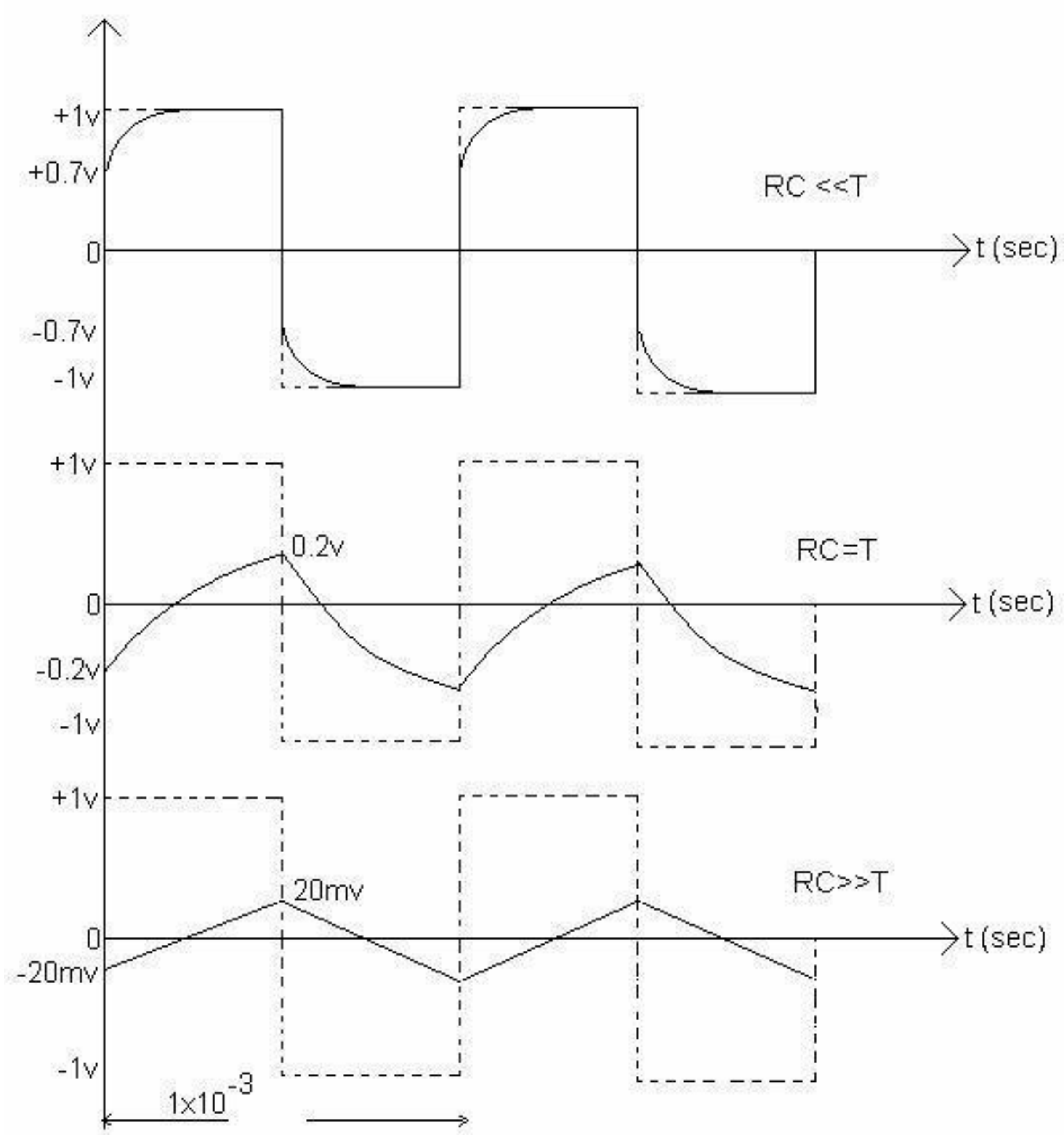
Calculation:

(a) RC = T

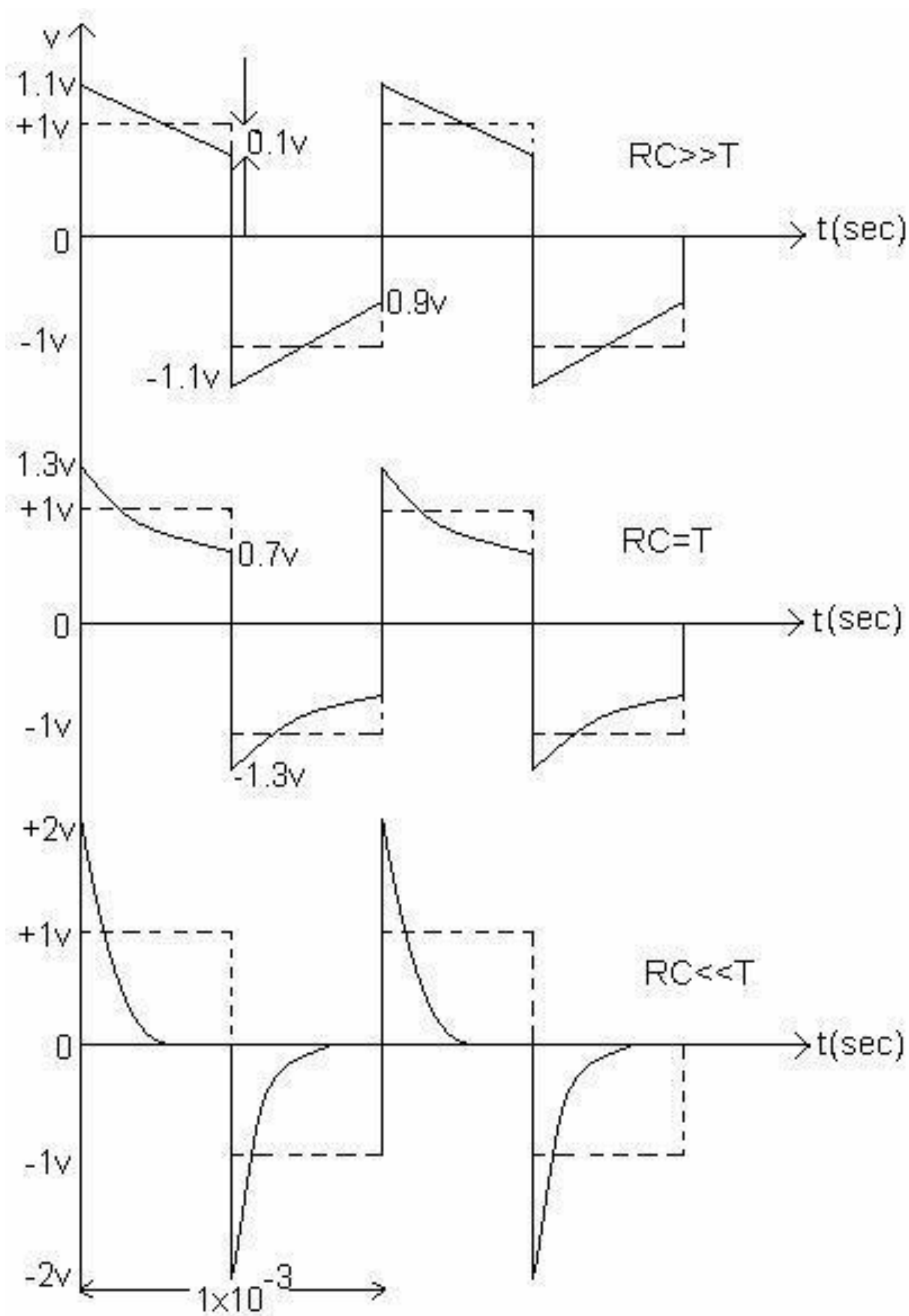
(b) RC<<T

(c) RC>>T

LOW PASS RC CIRCUIT:



HIGH PASS RC CIRCUIT:



PRECAUTIONS:

1. Connections should be made carefully.
2. Verify the circuit connections before giving supply.
3. Take readings without any parallax error.

Result:

RC low pass and high pass circuits are designed, frequency response and response at different time constants is observed.

Viva Questions:

1. Define linear wave shaping?
2. When does the low pass circuit act as integrator?
3. When does the high pass circuit acts as a differentiator?

Exercise Questions:

1. Design an ideal 1 micro second pulse is fed to an amplifier and draw output wave form under the following conditions: the upper 3db frequency is a) 10MHZ b) 1MHZ c) 0.1MHZ.

OBSERVATIONS:

EXPERIMENT NO-2

NON LINEAR WAVE SHAPPING-CLIPPERS

AIM: To obtain the output and transfer characteristics of various diode clipper circuits.

APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	4.7KΩ	1
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires		As Required
5	Diode	1N4007	2
6	DC Regulated power supply	0-30V,1A	1

THEORY:

The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

CIRCUIT DIAGRAMS:

POSITIVE PEAK CLIPPER WITH REFERENCE VOLTAGE, V=2V

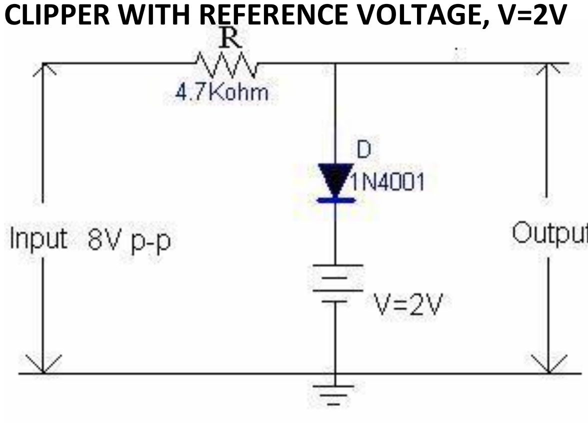


Fig.1

POSITIVE BAISE CLIPPER WITH REFERENCE VOLTAGE, V=2V

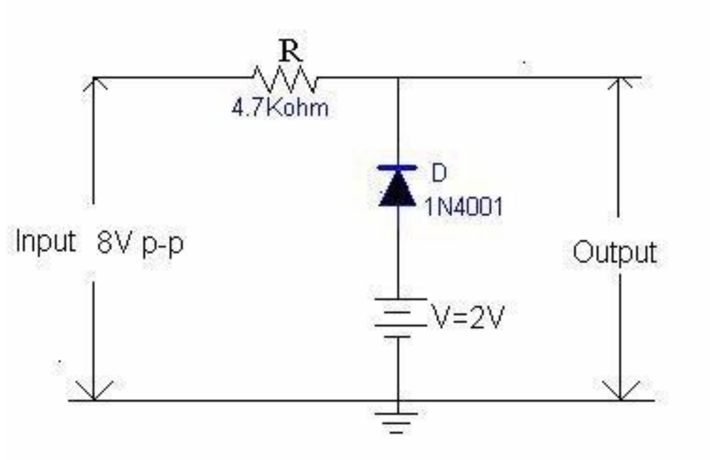


Fig.2

NEGATIVE BAISE CLIPPER WITH REFERENCE VOLTAGE, V=-2V

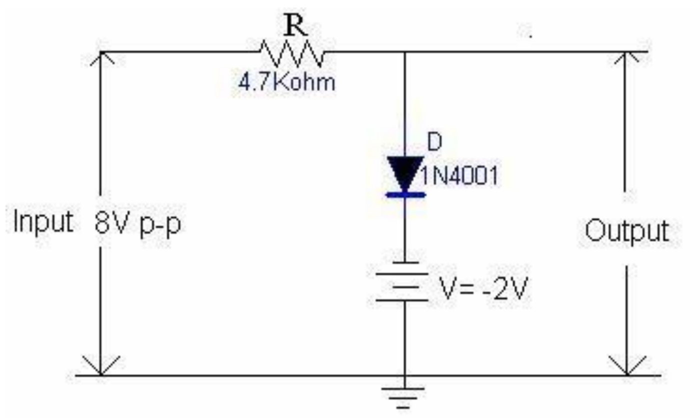


Fig.3

NEGATIVE PEAK CLIPPER WITH REFERENCE VOLTAGE, V=-2V

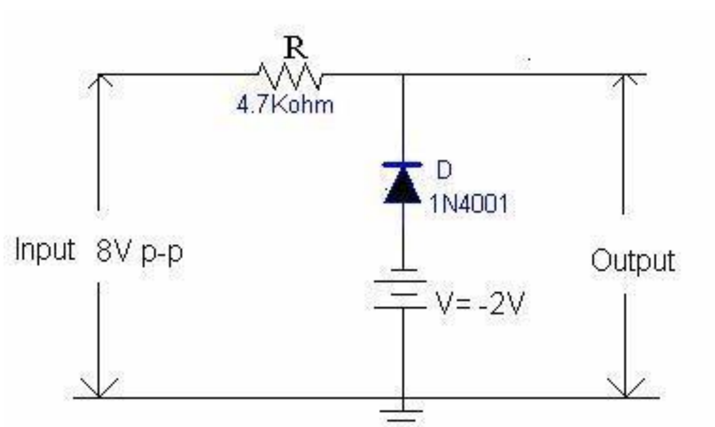


Fig.4

CLIPPING AT TWO INDEPENDENT LEVELS :(SLICCER)

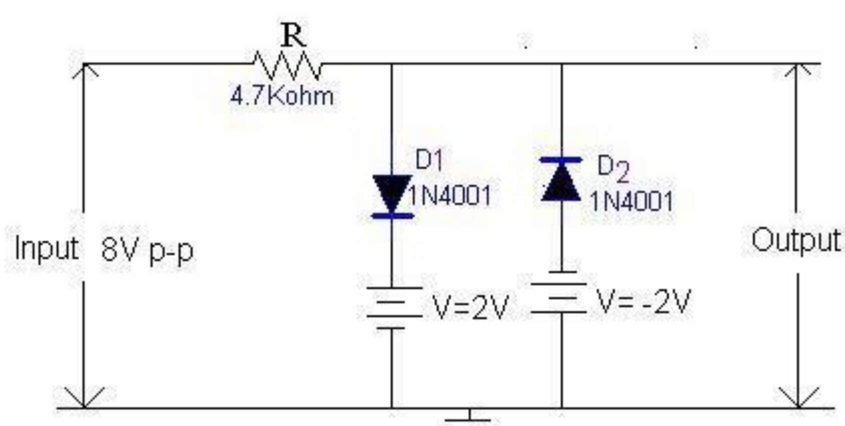


Fig.5

PROCEDURE:

1. Connect the circuit as per circuit diagram shown in Fig.1
2. Obtain a sine wave of constant amplitude 8 V p-p from function generator and apply as input to the circuit.
3. Observe the output waveform and note down the amplitude at which clipping occurs.
4. Draw the observed output waveforms.
5. To obtain the transfer characteristics apply dc voltage at input terminals and vary the voltage insteps of 1V up to the voltage level more than the reference voltage and note down the corresponding voltages at the output.
6. Plot the transfer characteristics between output and input voltages.
7. Repeat the steps 1 to 5 for all other circuits.

THEORETICAL CALCULATIONS:

Positive peak clipper:

V_r=2v, $V\gamma$=0.6v
When the diode is forward biased $V_o = V_r + V\gamma$ = 2.6v
When the diode is reverse biased the $V_o=V_i$

Positive base clipper:
V_r=2v, $V\gamma$=0.6v
When the diode is forward biased $Vo=Vr - V\gamma$ = 1.4v
When the diode is reverse biased $V_o=V_i$.

Negative base clipper:

V_r=2v, $V\gamma$=0.6v
When the diode is forward biased $V_o = -V_r + V\gamma$ = -1.4v
When the diode is reverse biased $V_o=V_i$.

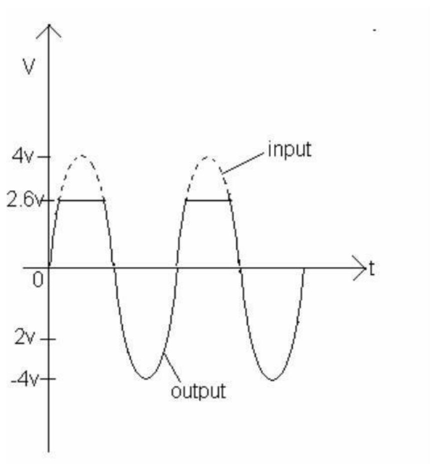
Negative peak clipper:
V_r=2v, $V\gamma$=0.6v
When the diode is forward biased V_o= -(V_r+ $V\gamma$) =-2.6v
When the diode is reverse biased V_o=V_i .

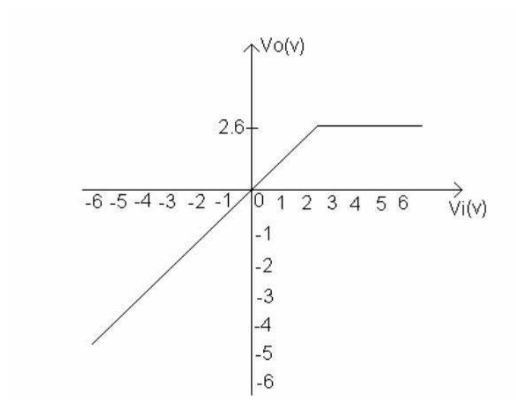
Slicer:

When the diode D1 is forward biased and D2 is reverse biased Vo= Vr+ V γ =2.6v
When the diode D2 is forward biased and D2 is reverse biased Vo=-(Vr+ Vγ) =-2.6v
When the diodes D1 &D2 are reverse biased Vo=Vi .

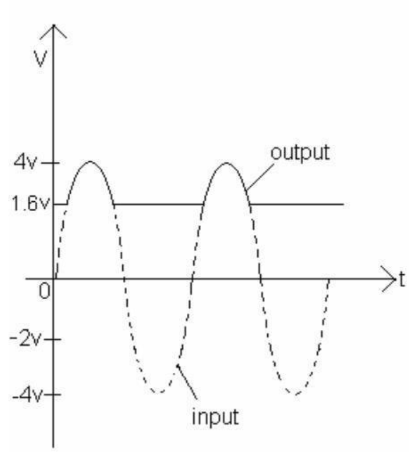
MODEL WAVE FORMS AND TRANSFER CHARACTERISTICS

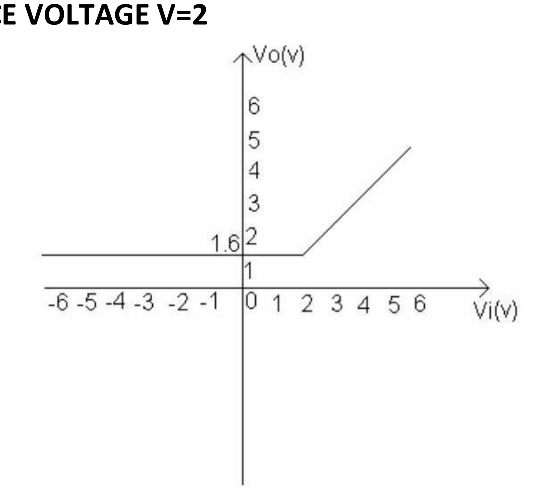
POSITIVE PEAK CLIPPER: REFERENCE VOLTAGE V=2V



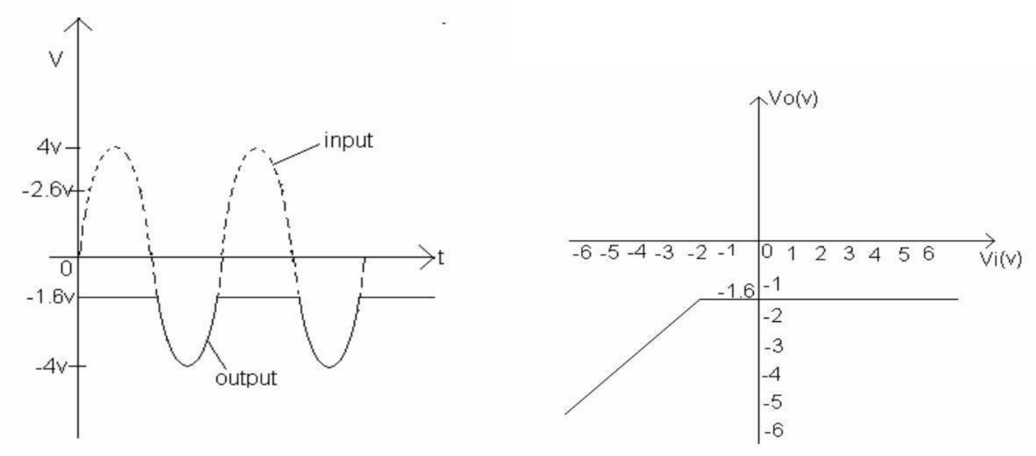


POSITIVE BASE CLIPPER: REFERENCE VOLTAGE V=2

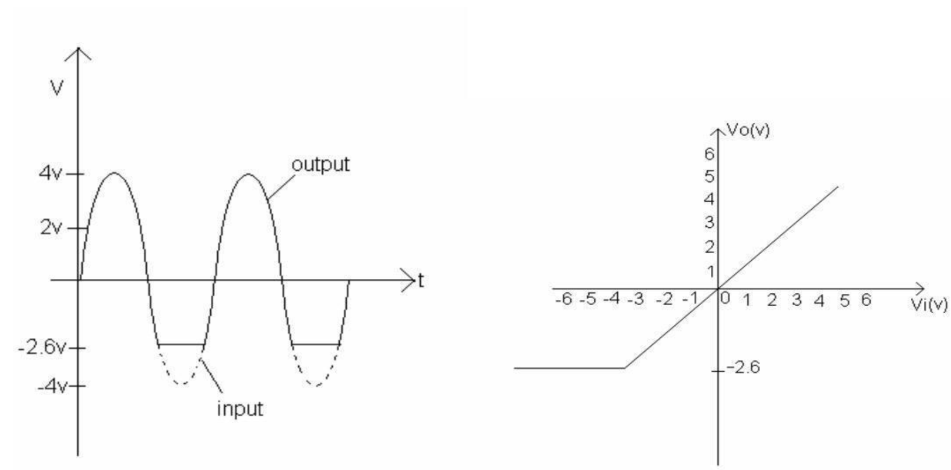




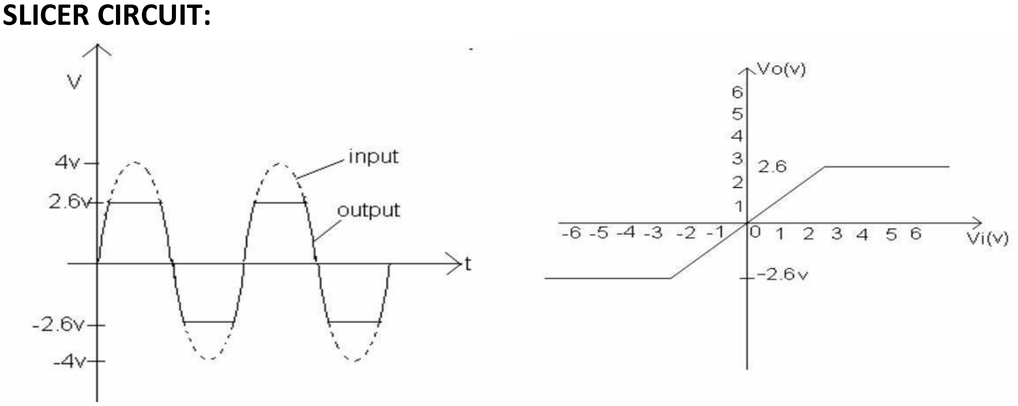
NEGATIVE BASE CLIPPER: REFERENCE VOLTAGE V=2V



NEGATIVE PEAK CLIPPER: REFERENCE VOLTAGE V=2V



SLICER CIRCUIT:



PRECAUTIONS:

1. Connections should be made carefully.
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

RESULT:

Performance of different clipping circuits is observed and their transfer characteristics are obtained.

VIVA:

1. In the fig.1 if reference voltage is 0v then what will be the output?
2. What are the other names for the clippers?

Exercise Questions:

1) Determine V_O for the network shown in Figure.1 for the given 16V P-P sine wave input. Also sketch the transfer characteristics. (Assume ideal diodes)

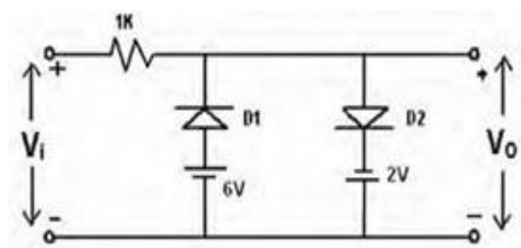
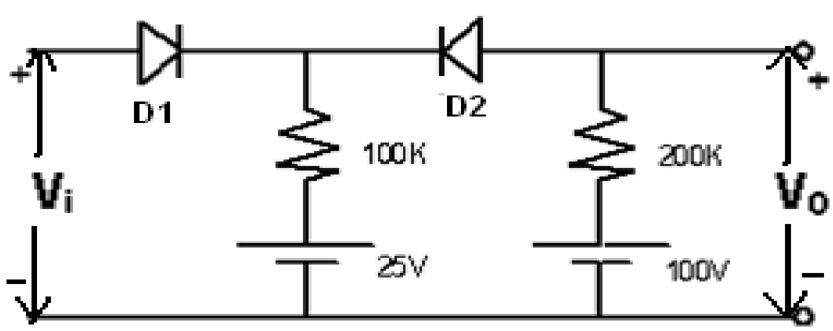


Figure.1

2) For the circuit shown in Figure.1, a sine wave input of 100V peak is applied. Sketch the output voltage V_O to the same time scale & transfer characteristic. Assume ideal diodes.



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OBSERVATIONS:

EXPERIMENT NO-3
NON LINEAR WAVE SHAPPING-CLAMPERS

AIM: To verify the output of different diode clamping circuits.

APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	100KΩ,1kΩ	1
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires	-	As Required
5	Diode	1N4007	1
6	DC Regulated power supply	0-30V,1A	1
7	Capacitor	0.1pF	1

THEORY:

"A clamping circuit is one that takes an input waveform and provides an output that is a faithful replica of its shape but has one edge tightly clamped to the zero voltage reference point". The circuits which are used to add a d.c level as per the requirement to the a.c signals are called clamper circuits. Capacitor, diode, resistor are the three basic elements of a clamper circuit. The clamper circuits are also called d.c restorer or d.c inserter circuits. The clampers are classified as (a) Negative clampers (b) Positive clampers

CIRCUIT DIAGRAMS

POSITIVE PEAK CLAMPING TO 0V:

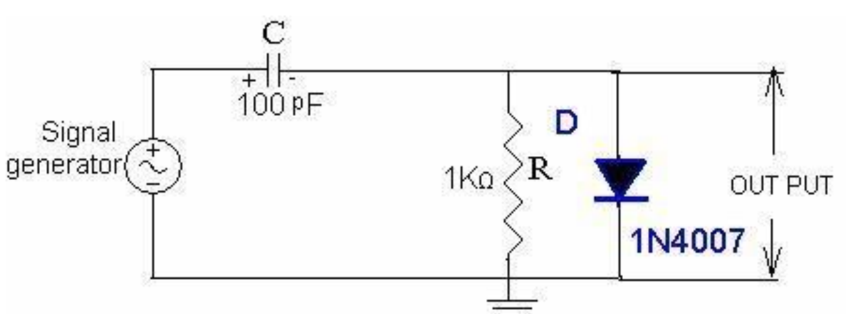


Fig.1

POSITIVE PEAK CLAMPING TO V_R=2V

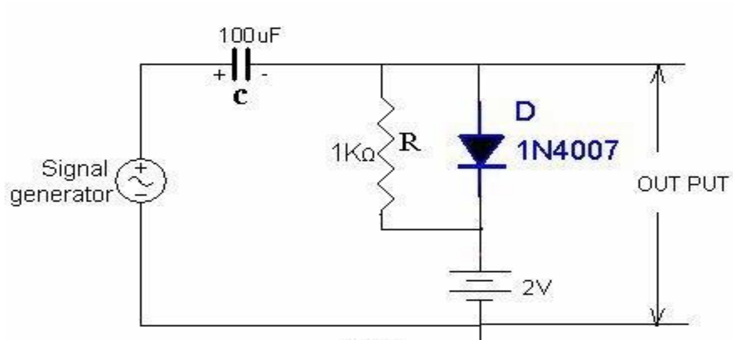


Fig.2

NEGATIVE PEAK CLAMPING TO V_R=0V

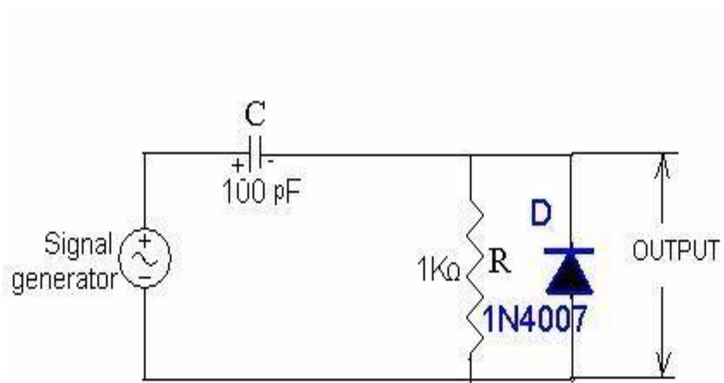


Fig.3

NEGATIVE PEAK CLAMPING TO V_R= -2V

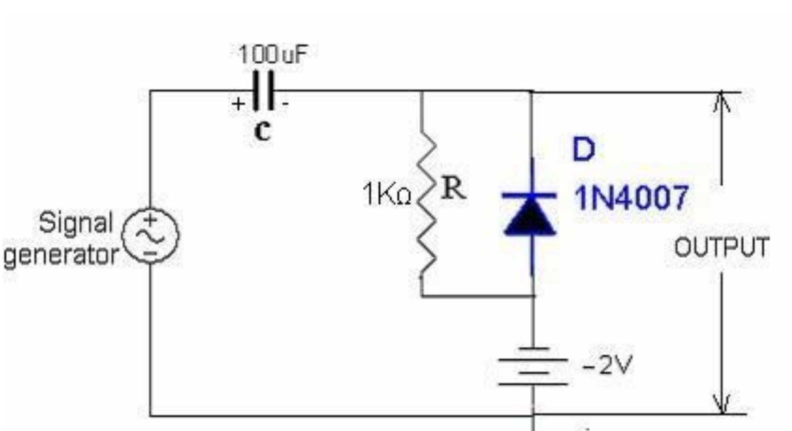


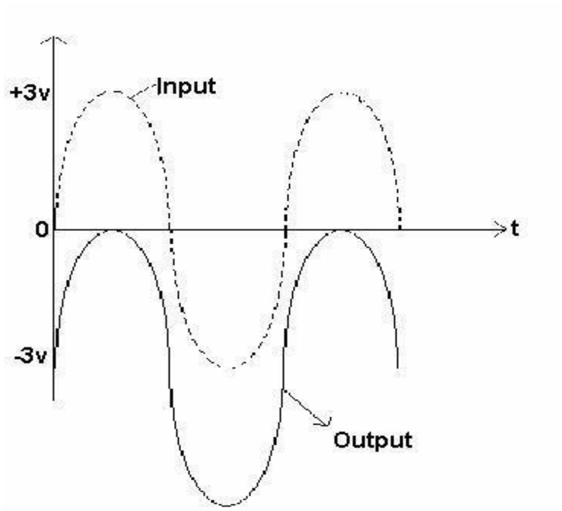
Fig.4

PROCEDURE:

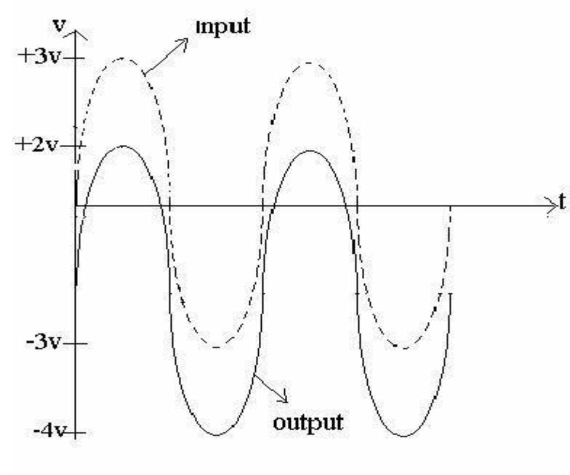
1. Connect the circuit as per circuit diagram.
2. Obtain a constant amplitude sine wave from function generator of 6 Vp-p, frequency of 1 KHz and give the signal as input to the circuit.
3. Observe and draw the output waveform and note down the amplitude at which clamping occurs.
4. Repeat the steps 1 to 3 for all circuits.

MODEL WAVEFORMS:

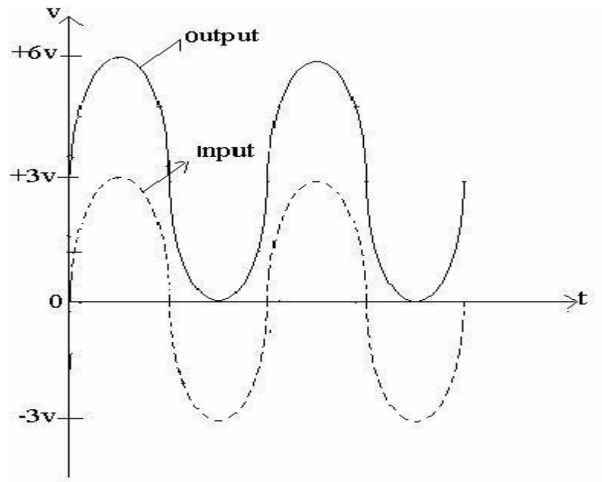
POSITIVE PEAK CLAMPING TO 0V:



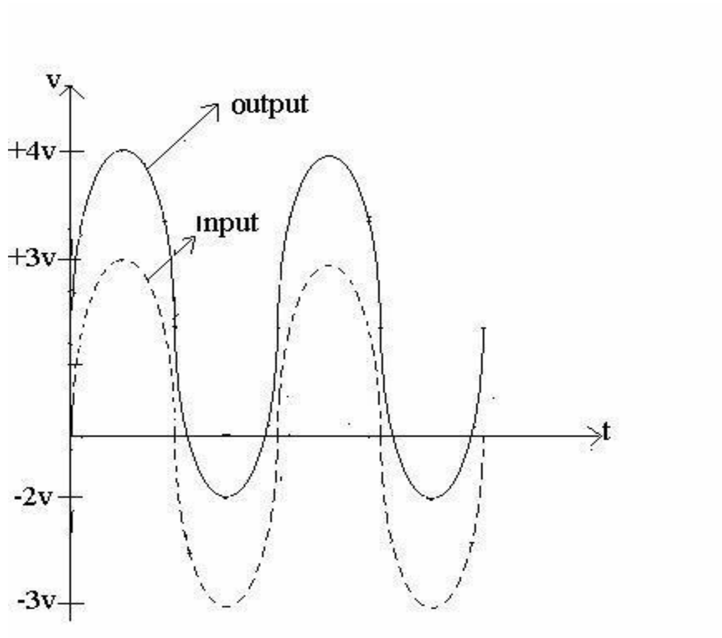
POSITIVE PEAK CLAMPING TO V_R=2



NEGATIVE PEAK CLAMPING TO 0V



NEGATIVE PEAK CLAMPING TO VR= -2V



PRECAUTIONS:

1. Connections should be made carefully.
2. Verify the circuit before giving supply.

Take readings without any parallax error.

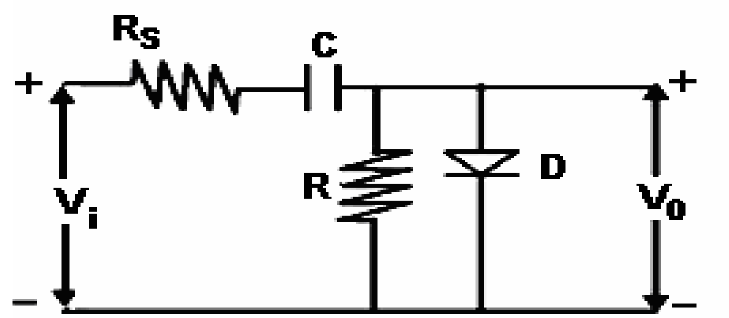
RESULT: Different clamping circuits are constructed and their performance is observed.

QUESTIONS

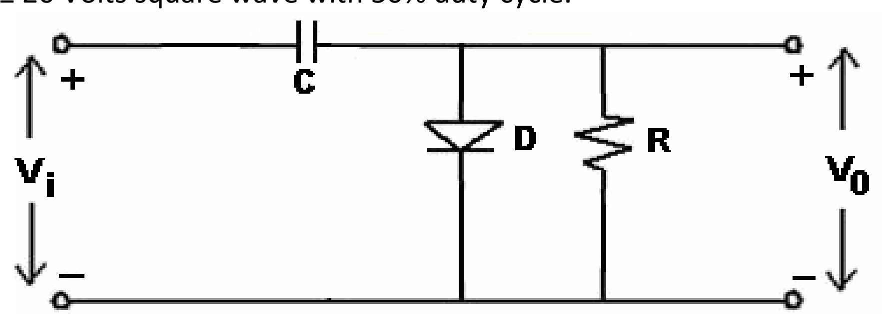
1. What is a clamper?
2. Give some practical applications of clamper.
3. What is the purpose of shunt resistance in clamper?

Exercise Questions:

1) a) A square wave input of period T = 1000 μ sec, Vpeak = 10V and Duty cycle = 0.2 is applied to the circuit shown in figure.2. Given, R_S = 100Ω, C = 1μF, R = 10K & Diode forward resistance, R_f = 100Ω.



2) Sketch the steady state output voltage for the clamper circuit and locate the output d.c level and the zero level. The diode used has R_f = 1KΩ, R_r = 600 KΩ, V_γ = 0. C = 0.1μF and R = 20 KΩ. The input is a ± 20 Volts square wave with 50% duty cycle.



OBSERVATIONS:

EXPERIMENT NO-4
TRANSISTOR AS A SWITCH

AIM: To obtain characteristics of a transistor as a switch.

APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	1KΩ	2
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires	-	As Required
6	DC Regulated power supply	0-30V,1A	1
7	Capacitor	1uF	1
8	Transistor	BC 107	1

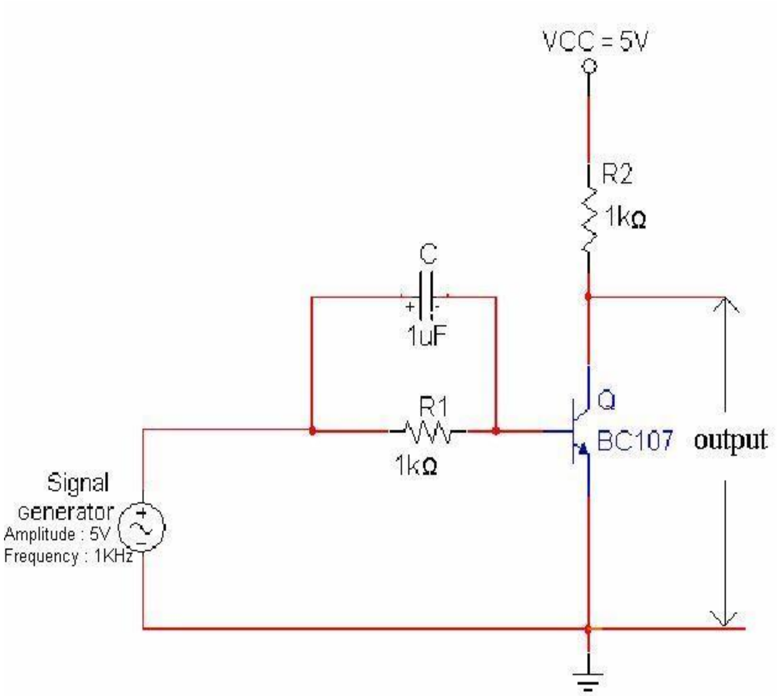
THEORY:

Transistors are widely used in digital logic circuits and switching applications. In these applications the voltage levels periodically alternate between a “LOW” and a “HIGH” voltage, such as 0V and +5V. In switching circuits, a transistor is operated at cutoff for the OFF condition, and in saturation for the ON condition. The active linear region is passed through abruptly switching from cutoff to saturation or vice versa. In cutoff region, both the transistor junctions between Emitter and Base and the junction between Base and Collector are reverse biased and only the reverse current which is very small and practically neglected, flows in the transistor. In saturation region both junctions are in forward bias and the values of V_{ce} (sat) and V_{be} (sat) are small.

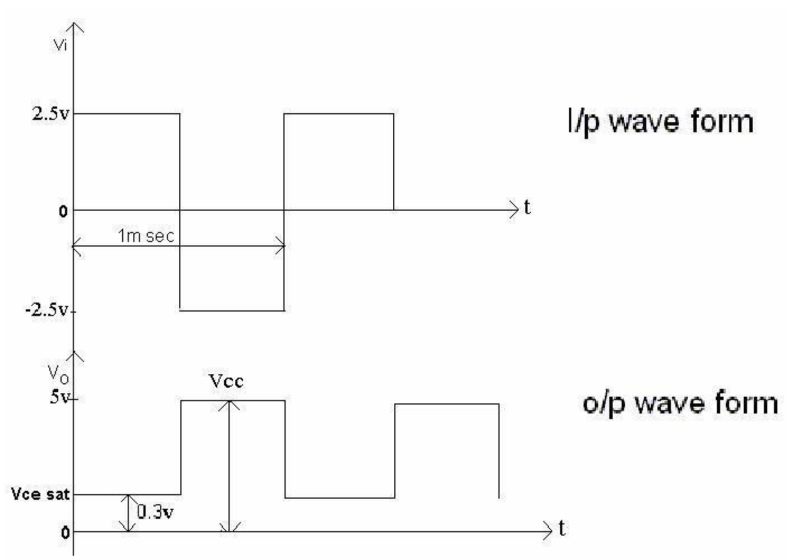
PROCEDURE:

1. Connect the circuit as per circuit diagram.
2. Obtain a constant amplitude square wave from function generator of 5V p-p and give the signal as input to the circuit.
3. Observe the output waveform and note down its voltage amplitude levels.
4. Draw the input and output waveforms

CIRCUIT DIAGRAM:



Model graph



THEORETICAL CALICULATIONS:

When Vi= +2.5v, the transistor goes into saturation region.
So $V_O = V_{ce\ sat} = 0.3V$.
When V_i=-2.5v, the transistor is in cutoff region so V_o=Vcc=5v

PRECAUTIONS:

1. Connections should be made carefully.
2. Verify the circuit before giving supply voltage.
3. Take readings without any parallax error.

RESULT:

Switching characteristics of a transistor are observed.

QUESTION & ANSWERS:

1. What are the limitations of transistor switch?
2. What is the turn on time of a transistor?

Exercise Questions:

1) For a C.E transistor circuits with V_{CC}=15V R_C=1.5KΩ.Caculate the transistor power dissipation a) at cutoff and b) at saturation

OBSERVATIONS:

EXPERIMENT NO-5
BISTABLE MULTIVIBRATOR

Aim: To observe the stable states voltages of Bi-stable Multivibrator.

Apparatus required

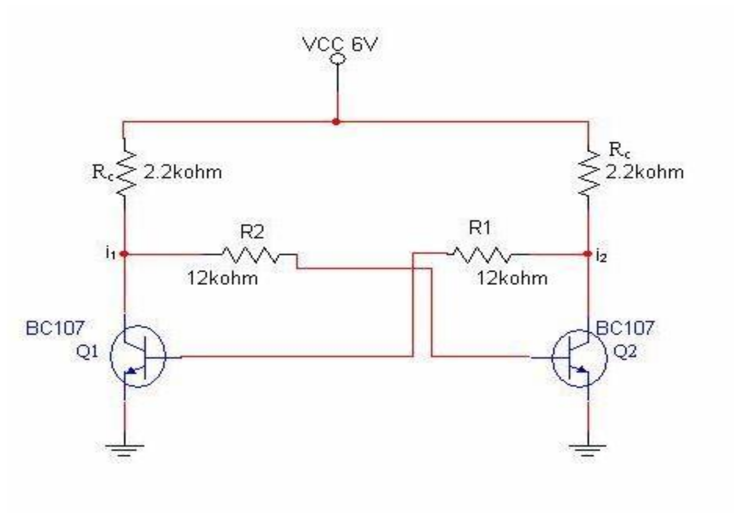
S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	2.2KΩ, 12KΩ	2
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires	-	As Required
6	DC Regulated power supply	0-30V,1A	1
8	Transistor	BC 107	2

THEORY:

The circuit diagram of a fixed bias Bi-stable multivibrator using transistors. The output of each amplifier is direct coupled to the input of the other amplifier. In one of the stable states transistor Q_1 and Q_2 is off and in the other stable state. Q_1 is off and Q_2 is on even though the circuit is symmetrical; it is not possible for the circuit to remain in a stable state with both the transistors conducting simultaneously and caring equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents i_1 and i_2 suppose there is a minute fluctuation in the current i_1-let us say it increases by a small amount.

Then the voltage at the collector of q_1 decreases. This will result in a decrease in voltage at the base of q_2. So q_2 conducts less and i_2 decreases and hence the potential at the collector of q_2 increases. This result in an increase in the base potential of q1.So q_1 conducts still more and i_1 is further increased and the potential at the collector of q_1 is further decreased, and so on. So the current i_1 keeps on increasing and the current i_2 keeps on decreasing till q_1 goes in to saturation and q_2 goes in to cut-off. This action takes place because of the regenerative feed – back incorporated into the circuit and will occur only if the loop gain is greater than one.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in figure.
2. Verify the stable state by measuring the voltages at two collectors by using multimeter.
3. Note down the corresponding base voltages of the same state (say state-1).
4. To change the state, apply negative voltage (say-2v) to the base of on transistor or positive voltage to the base of transistor (through proper current limiting resistance).
5. Verify the state by measuring voltages at collector and also note down voltages at each base.

PRECAUTIONS:

1. Connections should be made carefully.
2. Note down the parameters carefully.
3. The supply voltage levels should not exceed the maximum rating of the transistor.

RESULT: The stable state voltages of a Bi-stable multivibrator are observed.

QUESTION & ANSWERS:

1. What do you mean by a bistable circuit?
2. What are the other names of a bistable multivibrator?
3. What do you mean by triggering signal?

Exercise Questions:

1) A self-biased binary uses n-p-n transistors have maximum values of V_{CE} (sat) =0.4V and V_{BE} (sat) = 0.8V and V_{BE} cutoff = 0V. The circuit parameters are V_{CC} = 15V, R_C = 1KΩ, R_1 = 6KΩ, R2 = 15KΩ and R_E = 500Ω.

a) Find the stable-state currents and voltages.

OBSERVATIONS:

EXPERIMENT NO-6
ASTABLE MULTIVIBRATOR

AIM: To Observe the ON & OFF states of Transistor in an Astable Multivibrator.

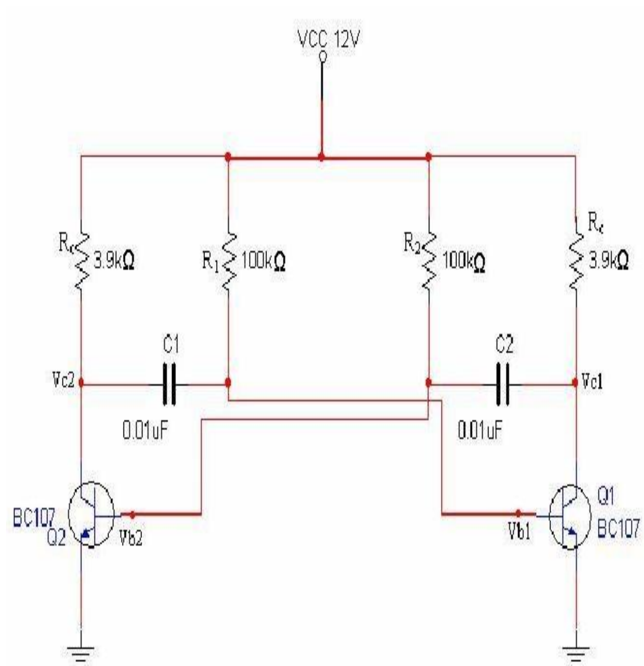
APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	3.9KΩ, 100KΩ	2
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires	-	As Required
6	DC Regulated power supply	0-30V,1A	1
8	Transistor	BC 107	2
	Capacitor	0.01 µF	2

THEORY:

An Astable Multivibrator has two quasi stable states andit keeps on switching between these two statesby itself . No external triggering signal is needed. The astable multivibrator cannot remain indefinitely in any one of the two states .The Two amplifier stages of an astable multivibrator are regenerative across coupled by Capacitors. The astable multivibrator may be to generate a square wave of period, 1.38RC

CIRCUIT DIAGRAM



PROCEDURE:

1. Calculate the theoretical frequency of oscillations of the circuit.
2. Connect the circuit as per the circuit diagram.
3 Observe the voltage wave forms at both collectors of two transistors simultaneously.
4. Observe the voltage wave forms at each base simultaneously with corresponding collector voltage.
5. Note down the values of wave forms carefully.
6. Compare the theoretical and practical values.

CALCULATIONS:

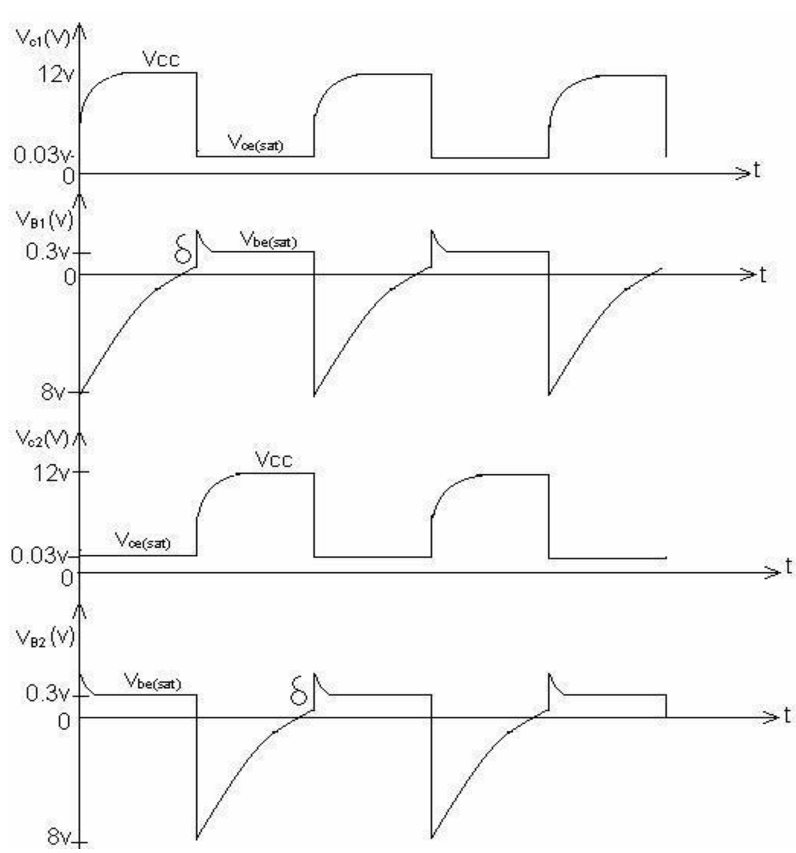
THEORITICAL VALUES:

RC= R_1C_1+ R_2C_2

Time Period, T = 1.368RC

Frequency, f = 1/T =

MODEL WAVEFORMS



PRECAUTIONS:

1. Connections should be made carefully.
2. Readings should be noted without parallax error.

RESULT:

The wave forms of astable multivibrator have been verified.

VIVA QUESTIONS :

1. Define stable state?
2. Define quasi stable state?

Exercise Questions:

1) Design a collector coupled astable multivibrator for the following specifications with Silicon transistor. IC (sat) = 10m A; hfe (min) = 20; VCC =10V; pulse width=10µsec; duty Cycle=40%

OBSERVATIONS:

EXPERIMENT NO-7
MONOSTABLE MULTIVIBRATOR

AIM: To observe the stable state and quasi stable state voltages in monostable Multivibrator.

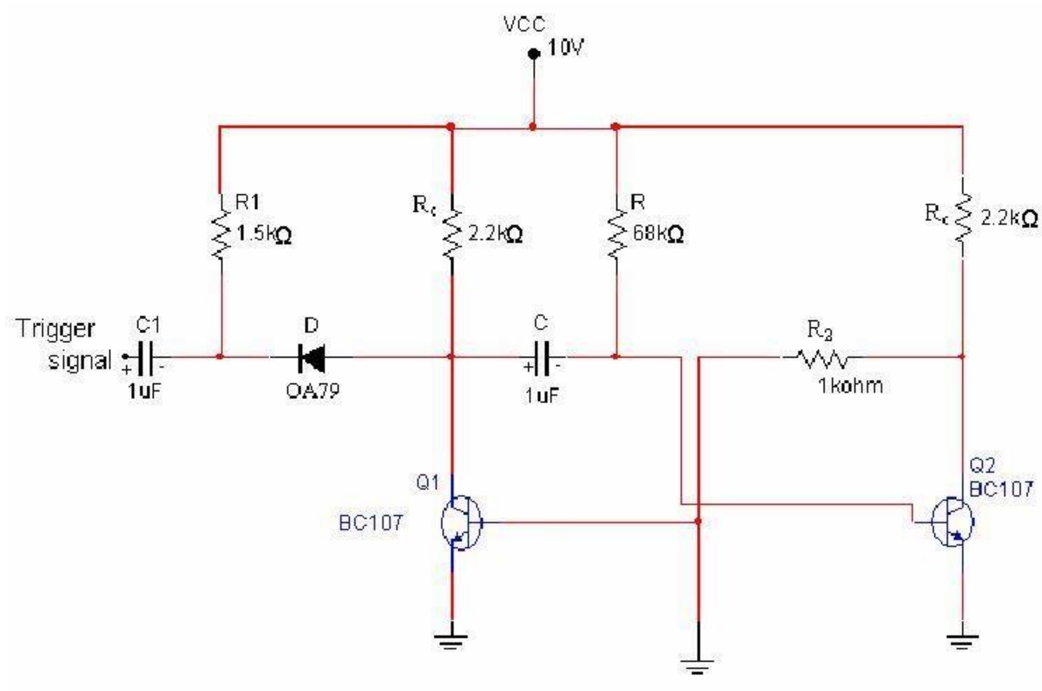
APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	1KΩ	1
		68KΩ	1
		2.2KΩ	1
		1.5KΩ	1
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires	-	As Required
6	DC Regulated power supply	0-30V,1A	1
8	Transistor	BC 107	2
	Capacitor	1 µF	2
	Diode	IN4007	1

THEORY:

A monostable multivibrator on the other hand compared to astable, bistable has only one stable state, the other state being quasi stable state. Normally the multivibrator is in stable state and when an externally triggering pulse is applied, it switches from the stable to the quasi stable state. It remains in the quasi stable state for a short duration, but automatically reverse switches back to its origional stable state without any triggering pulse. The monostable multivibrator is also referred as ‘one shot’ or ‘uni vibrator’ since only one triggering signal is required to reverse the original stable state. The duration of quasi stable state is termed as delay time (or) pulse width (or) gate time. It is denoted as‘t’.

CIRCUIT DIAGRAM:



PROCEDURE:

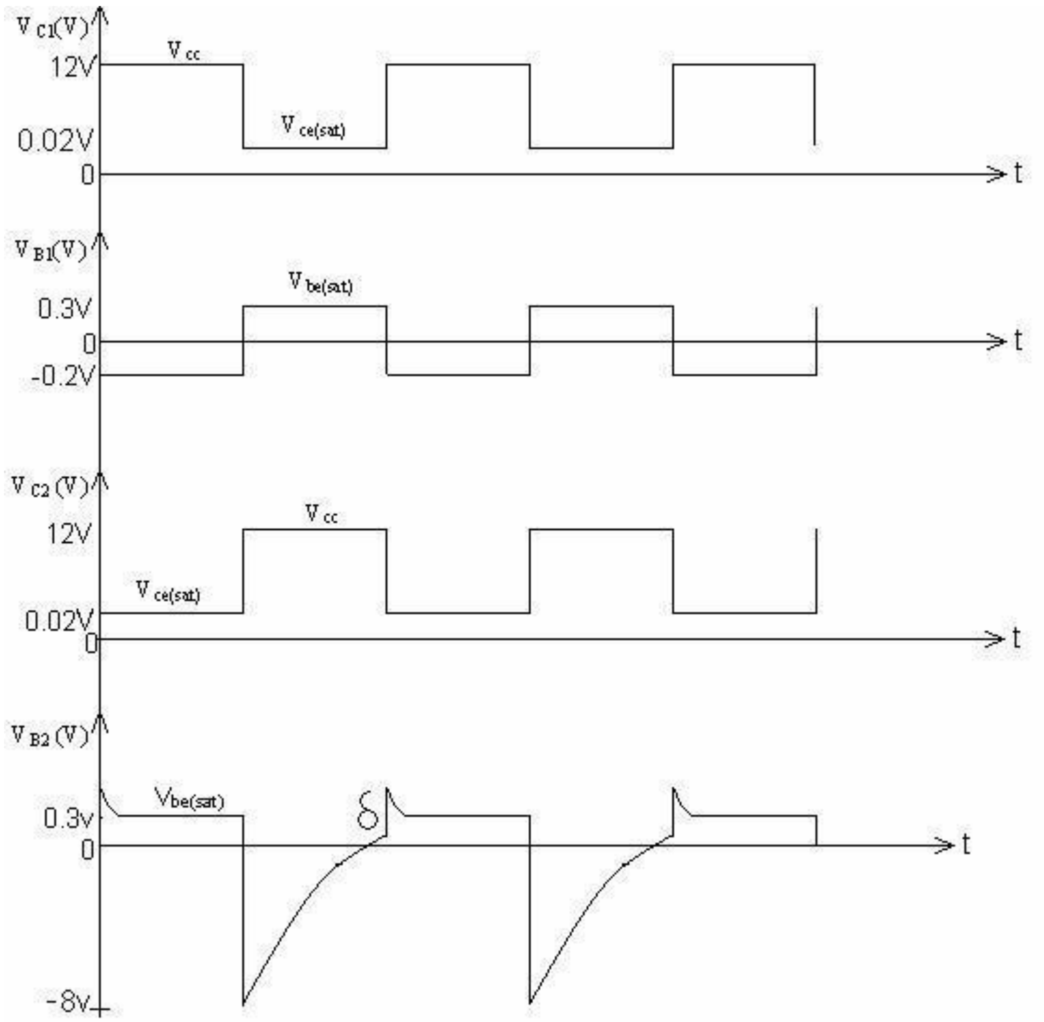
1. Connect the circuit as per the circuit diagram.
2. Verify the stable states of Q_1 and Q_2
3. Apply the square wave of 2v p-p , 1KHz signal to the trigger circuit.
4. Observe the wave forms at base of each transistor simultaneously.
5. Observe the wave forms at collectors of each transistor simultaneously.
6. Note down the parameters carefully.
7. Note down the time period and compare it with theoretical values.
8. Plot wave forms of V_{b1}, V_{b2}, V_{c1} & V_{c2} with respect to time .

CALCULATIONS:

Theoretical Values:
Time Period, T = 0.693RC

Frequency, f = 1/T =

MODEL WAVEFORMS:



PRECAUTIONS:

1. Connections should be made carefully.
2. Note down the parameters without parallax error.
3. The supply voltage levels should not exceed the maximum rating of the transistor.

RESULT:

Stable state and quasi stable state voltages in monostable multivibrator are observed

QUESTION & ANSWERS:

1. What are the other names of Mono Stable multivibrator?
2. Which type of triggering is used in mono stable multi vibrator?
3. Define transition time?

Exercise Questions:

1) Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with h_{FE} (min) =20. In stable State, the transistor in cut-off has V_{BE} = -1V and the transistor in saturation has base current, I_B which is 50% excess of the I_B (min) value. Assume V_{CC} = 8V, I_C (sat) =2mA, delay time = 2.5ms &; $R_1 = R_2$. Find R_C, R, R_1, C and V_{BB}.

OBSERVATIONS:

EXPERIMENT NO-8
UJT RELAXATION OSCILLATOR

AIM: To obtain the characteristics of UJT Relaxation Oscillator.

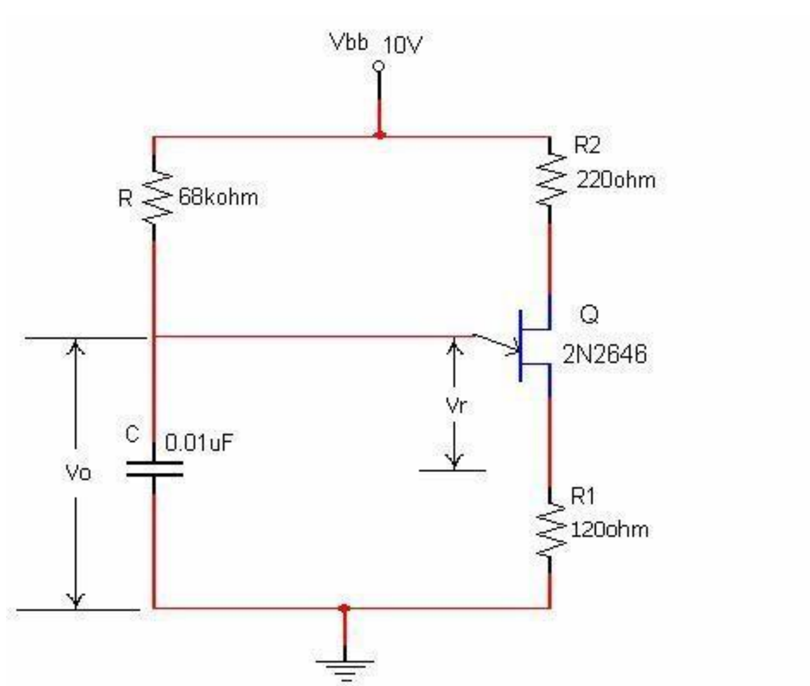
APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	220Ω	1
		68KΩ	1
		120Ω	1
2	CRO	20MHz	1
4	Connecting Wires	-	As Required
6	DC Regulated Power Supply	0-30V,1A	1
	Capacitor	0.01 µF	1
	UJT	2N 2646	

THEORY:

Many devices such as transistor,UJT, FET can be used as a switch. Here UJT is used as a switch to obtain the sweep voltage. Capacitor C charges through the resistor towards supply Voltage,V_{bb}. As long as the capacitor voltage is less than peak Voltage,V_p, the emitter appears as an open circuit. $\mathbf{V_p = \eta V_{bb} + V_\gamma}$

CIRCUIT DIAGRAM:



DESIGN EQUATIONS:

THEORETICAL CALCULATIONS

$V_p = V_\gamma+(R_1/ R_1 R_2)V_{bb}$
=0.7+(120/120+220)10
=8.57V

1. When C=0.1µF
T_c =RC ln(V_{bb}- V_v/ V_{bb}- V_p) =(68K) (0.1µF) (12/12-8.57)
= 3.6ms
T_d =R_1C=(120)(0.1µ)=12 µsec.

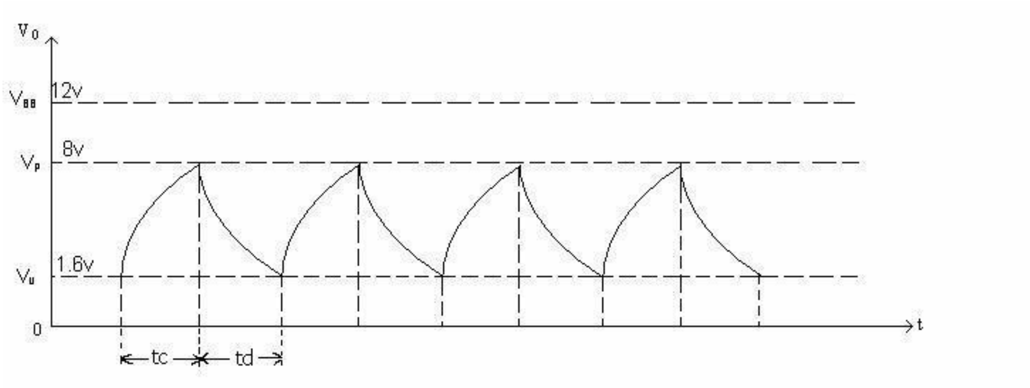
2. When C=0.01µF
T_c =RC ln(V_{bb}- V_v/ V_{bb}- V_p)
=(68K) (0.01µF) (12/12-8.5)
= 365µs
T_d =R_1C=(120)(0.01µ)=1.2 µsec.

3. When C=0.001µF
Tc =RC ln (Vbb- Vv/ Vbb- Vp)
=(68K) (0.001µF) (12/12-8.5)
= 36.5µs
Td =R1C=(120)(0.01µ)=0.12 µsec

PROCEDURE:

1) Connect the circuit as shown in figA.
2) Observe the voltage waveform across the capacitor, C.
3) Change the time constant by changing the capacitor values to 0.1µF and 0.001 µF and observe the wave forms.
4) Note down the parameters, amplitude, charging and discharging periods of the wave forms
5) Compare the theoretical and practical time periods.
6) Plot the graph between voltages across capacitor with respect to time

MODEL GRAPH:



PRECAUTIONS:

1. Connections should be given carefully.
2. Readings should be noted without parallax error.

RESULT: Performance and construction of UJT Relaxation Oscillator is observed.

VIVA QUESTIONS:

1. What do you mean by a) voltage time base generator, b) a current time base generator?

OBSERVATIONS:

EXPERIMENT NO-9
SCHMITT TRIGGER

AIM: To generate a square wave from a given sine wave using Schmitt Trigger

APPARATUS REQUIRED

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	100Ω	1
		6.8KΩ	1
		3.90Ω	1
		3.3KΩ	1
		2.2KΩ	2
2	CRO	20MHz	1
3	Function generator	1MHz	1
4	Connecting Wires	-	As Required
6	DC Regulated power supply	0-30V,1A	1
8	Transistor	BC 107	2
	Capacitor	0.01 µF	1

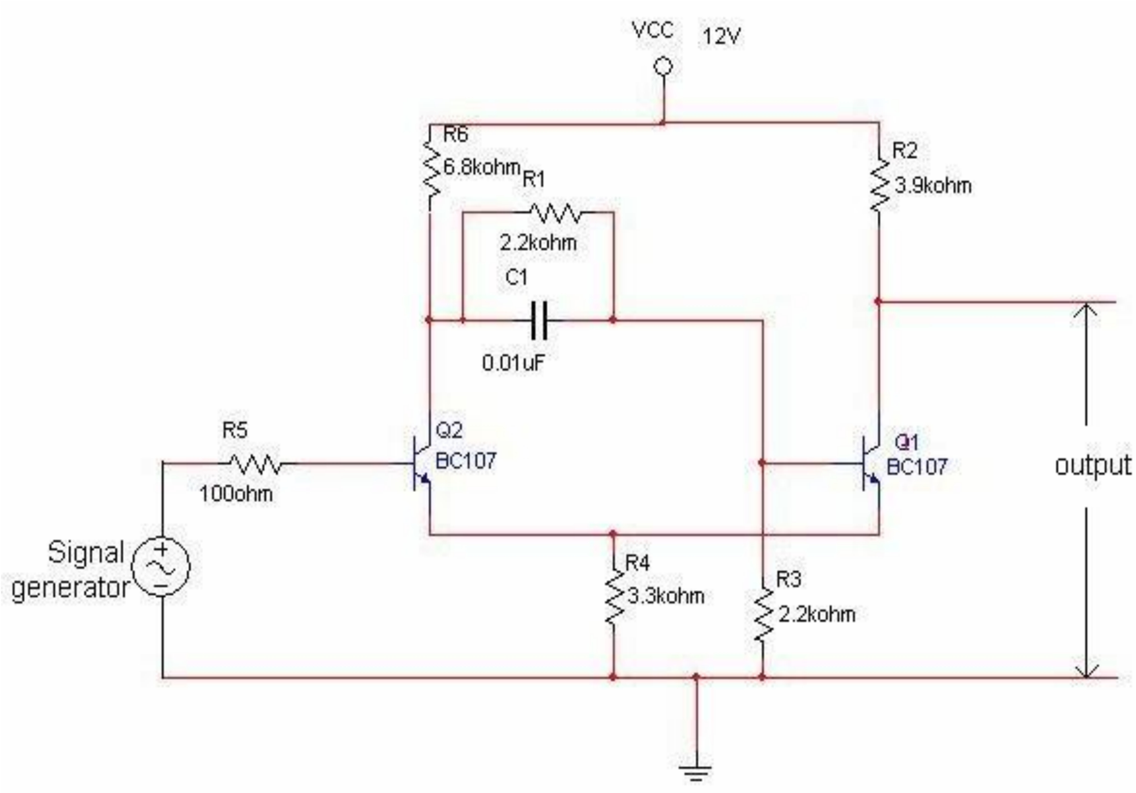
THEORY:

Schmitt trigger is a bistable circuit and the existence of only two stable states results form the fact that positive feedback is incorporated into the circuit and from the further fact that the loop gain of the circuit is greater than unity. There are several ways to adjust the loop gain. One way of adjusting the loop gain is by varying Rc1. Under quiescent conditions Q1 is OFF and Q2 is ON because it gets the required base drive from Vcc through Rc1 and R1. So the output voltage is Vo=Vcc-Ic2Rc2 is at its lower level. Untill then the output remains at its lower level.

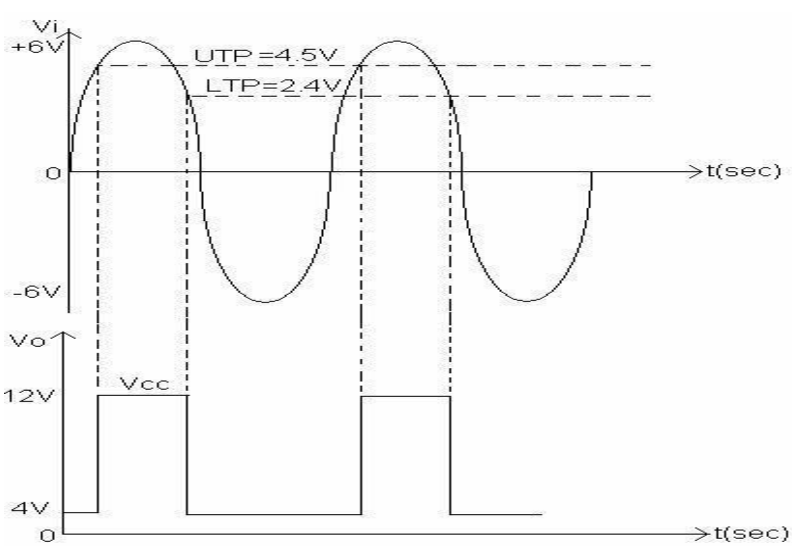
PROCEDURE:

1. Connect the circuit as per circuit diagram.
2. Apply a sine wave of peak to peak amplitude 10V, 1 KHz frequency wave as input to the circuit.
3. Observe input and output waveforms simultaneously in channel 1 and channel 2 of CRO.
4. Note down the input voltage levels at which output changes the voltage level.
5. Draw the graph between voltage versus time of input and output signals.

CIRCUIT DIAGRAM:



MODEL GRAPH:



PRECAUTIONS:

1. Connections should be made carefully.
2. Readings should be noted carefully without any parallax error.

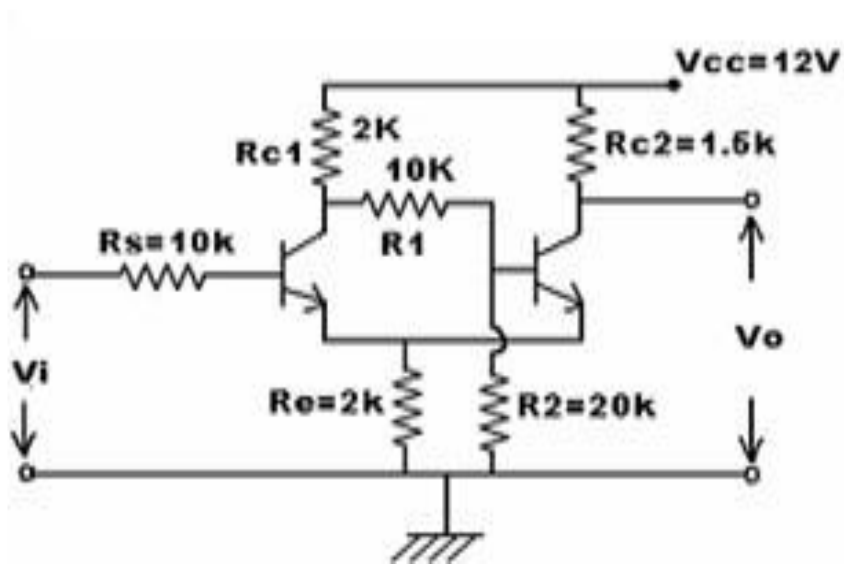
RESULT: Schmitt trigger is constructed and observed its performance.

VIVA QUESTIONS

1. What is the other name of the Schmitt trigger?
2. What are the applications of the Schmitt trigger?
3. Define the terms UTP & LTP?

Exercise Questions:

1. For the given circuit shown in Figure find UTP & LTP. Data given h_{fe} (min) = 40, V_{CE} (sat) = 0.1 V, V_{BE} (sat)=0.7 V, V_{γ} = 0.5V, V_{BE} (active) = 0.6V.



2. Design a Schmitt trigger circuit using n-p- n silicon transistors to meet the following specifications:
V cc =12V, UTP=4V, LTP=2V, h fe =60, I C2 =3mA. Use relevant assumptions and the empirical relationships.

OBSERVATIONS:

EXPERIMENT NO-10
STUDY OF LOGIC GATES

AIM: To construct the basic and universal gates using discrete components and Verify truth table.

APPARATUS REQUIRED:

S.No	Name of the Component/Equipment	Specifications	Quantity
1	Resistors	100Ω	1
		4.7KΩ	1
3	Bread Board		1
4	Connecting Wires	-	As Required
6	DC Regulated power supply	0-30V,1A	1
8	Transistor	BC 107	1
	Diode	IN4007	2
	LED	-	1

THEORY:

1. OR-GATE:

OR gate has two or more inputs and a single output and it operates in accordance with the following definitions. The output of an OR gate is high if one or more inputs are high. When all the inputs are low then the output is low. If two or more inputs are in high state then the diodes connected to these inputs conduct and all other diodes remain reverse biased so the output will be high and OR function is satisfied.

2. AND-GATE:

AND gate has two or more inputs and a single output and it operates in accordance with the following definitions. The output of an AND gate is high if all inputs are high. If Vr is chosen i.e. more positive than Vcd then all diodes will be conducting upon a coincidence and the output will be clamped at ‘1’. If Vr is equal to Vcd then all diodes are cut-off and output will raise to the voltage Vr if not all inputs have same high value then the output of AND gate is equal to Vi (min0).

3. NOT-GATE:

The NOT gate circuit has a single output and a single input and perform the operation of negation in accordance with definition, the output of a NOT gate is high if the input is low and the output is low or zero if the input is high or 1.

4. NOR-GATE:

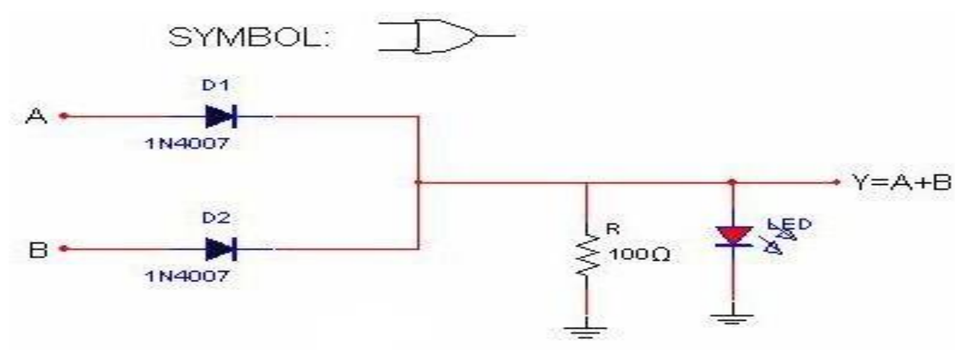
A negation following on OR is called as NOT-OR gate NOR gate. As shown in figure if Vo is applied as input signal to the diodes then both diodes are forward biased. Hence no voltage is applied to emitter base junction and total current is passed through the LED and it glows which indicate high or one state.

5. NAND-GATE:

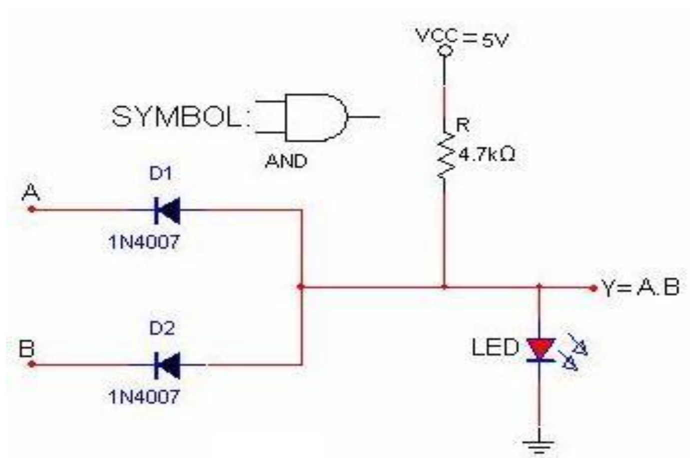
The NAND gate can be implemented by placing a transistor NOT gate after the AND gate circuit with diodes. These gates are called diode-transistor logic gates.
If Vo is applied to input of the diode then the diode D1 and D2 will be forward biased. Hence no voltage applied across base-emitter junction and this junction goes into cut-off region. Hence total current from source Vce will flow through LED and it flows which indicate the one state or high state.

CIRCUIT DIAGRAMS:

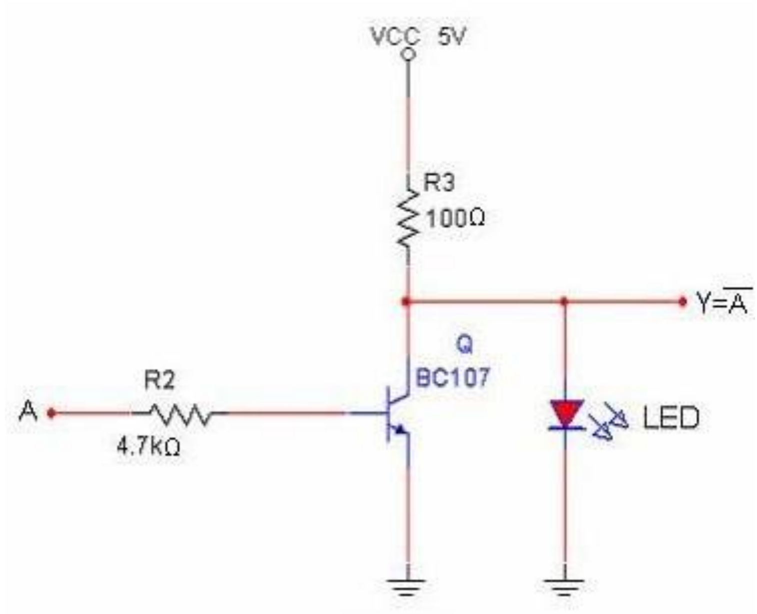
1. OR GATE



2. AND GATE



3.NOT GATE:



4.NOR GATE:

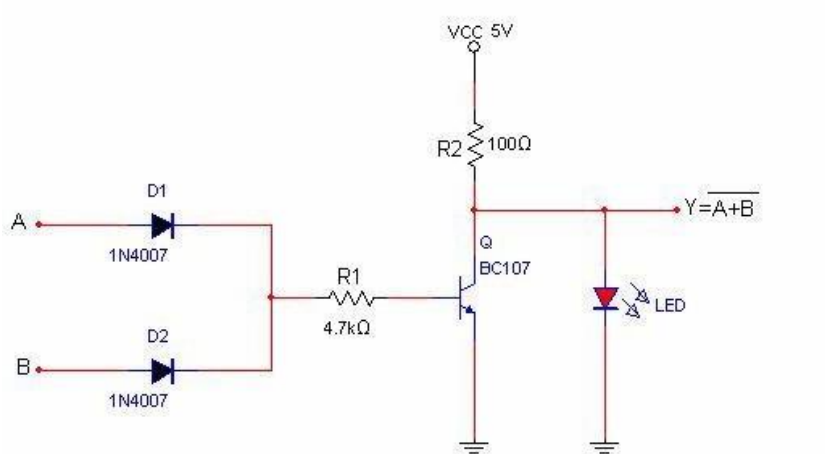
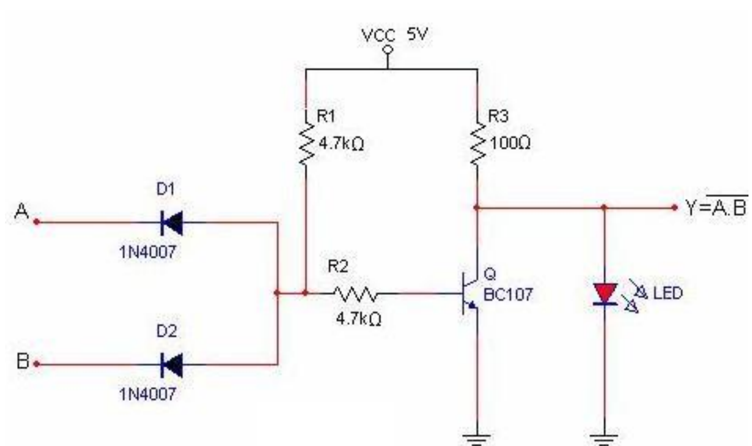


Fig.4

5.NAND GATE



TRUTH TABLES:

1.AND GATE:

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

2.OR GATE:

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT GATE:

NOT gate	
A	$\overline{A}$
0	1
1	0

4.NOR GATE

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

5. NAND GATE:

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Connect the circuit as per diagram.
2. Apply 5v from RPS for logic 1and 0v for logic 0.
3. Measure the output voltage using digital multimeter and verify the truth table.
4. Repeat the same for all circuits.

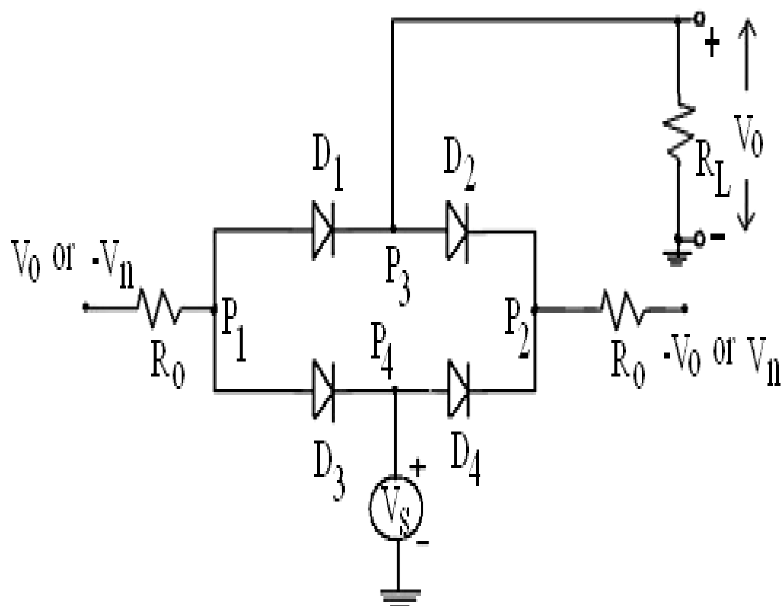
RESULT: Basic and universal gates are constructed using discrete components and their truth tables are verified.

VIVA QUESTIONS:

1. What are the universal gates? Why they are called universal gates?
2. What is the other name of the EX-NOR gate?

Exercise Questions:

1) For the four-diode sampling gate shown in figure.1, Vs = 25V, R_f = 50Ω, R_L = Rc =100KΩand R2 = 2KΩ. Find $(Vc)_{min}$, A, V_{min} and $(Vn)_{min}$ for V = V_{min}?



OBSERVATIONS: